

A 10-Gb/s Space Sampling Burst-Mode Clock and Data Recovery Circuit for Passive Optical Networks

Bhavin J. Shastri and David V. Plant

Photonic Systems Group, Dept. of Electrical and Computer Eng., McGill University, Montreal, QC H3A 2A7, Canada
shastri@ieee.org

Abstract—We demonstrate a novel 10-Gb/s burst-mode CDR circuit for PONs featuring instantaneous (0-bit) phase acquisition with $\text{BER} < 10^{-11}$. Our design is based on hybrid topology: feedback CDR and feed-forward clock phase aligner utilizing space-sampled clocks.

I. INTRODUCTION

Passive optical networks (PONs) are recognized as an economic solution to alleviate the bandwidth bottleneck in access networks by deploying fiber-to-the-home. The challenge in the design of a chip set for PONs arises from the upstream data path as the network is point-to-multipoint. Using time division multiple access, multiple optical network units (ONUs) transmit data to the optical line terminal (OLT) in the central office. Due to optical path differences, the data received at the OLT is inherently bursty with asynchronous phase steps $|\Delta\varphi| \leq 2\pi$ rad, that exist between the consecutive k^{th} and $(k+1)^{\text{th}}$ packet. This inevitably causes conventional clock and data recovery circuits (CDRs) to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDR feedback loop enough time to settle down and thus acquire lock. However, the use of a preamble introduces overhead, reducing the effective throughput and increasing delay. Consequently, to deal with bursty data, the OLT requires a burst-mode CDR (BM-CDR). The most important characteristic of the BM-CDR is its phase acquisition time which must be as short as possible. In this paper, we present a novel BM-CDR architecture based on a hybrid topology; that is, a combination of feedback and feed-forward. The BM-CDR provides instantaneous phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad with a bit-error rate (BER) $< 10^{-11}$.

II. NOVEL BM-CDR ARCHITECTURE

A block diagram of the proposed BM-CDR is shown in Fig. 1. The BM-CDR is composed of a phase-tracking CDR and a clock phase aligner (CPA). The CDR senses data D_{in} , and generates a synchronized clock CK , with a voltage-controlled oscillator (VCO) in a phase-locked (feedback) loop (PLL). The phase and frequency of CK is compared to D_{in} in the phase/frequency detector (PFD), generating an error signal that is passed through the charge pump (CP) and the low-pass filter (LPF) to set the voltage required by the VCO to oscillate at the frequency of interest.

Burst-mode functionality is obtained with the CPA which utilizes multi-phase clocks and a phase picking algorithm

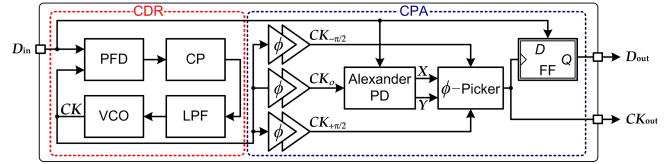


Fig. 1. BM-CDR architecture.

based on an “early-late” detection principle. This CPA is based on a feed-forward topology, and comprises of phase (ϕ -) shifters, an Alexander phase detector (PD), a ϕ -picker, and a D flip-flop (D-FF). The ϕ -shifters utilize the clock recovered by the CDR CK , to provide multiple clocks: CK_o , $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases: 0 rad, $-\pi/2$ rad, and $+\pi/2$ rad, respectively, with respect to CK . Next, an Alexander PD [1] which inherently exhibits *bang-bang* (binary) characteristics is used to strobe the data waveform D_{in} , with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions [see Fig. 2(a)], resulting in three data samples: previous bit A , current bit B , and a sample of the current bit at the zero crossing T . Depending on the phase difference between the consecutive packets, the PD aided by these samples, $X \equiv T \oplus B$ and $Y \equiv A \oplus T$, can determine the location of the clock edge with respect to the data edge as follows: (a) if $A \neq T = B$ ($X \downarrow$, $Y \uparrow$) $\Rightarrow CK_o$ lags D_{in} —is late—when $-\pi < \Delta\varphi < 0$ rad [see Fig. 2(b)]; (b) if $A = T \neq B$ ($X \uparrow$, $Y \downarrow$) $\Rightarrow CK_o$ leads D_{in} —is early—when $0 < \Delta\varphi < +\pi$ rad [see Fig. 2(c)]; (c) if $A = T = B$ ($X \downarrow$, $Y \downarrow$) \Rightarrow no data transition is present due to consecutive identical digits (CIDs) and (d) if $A = B \neq T$ ($X \uparrow$, $Y \uparrow$) \Rightarrow no decision is possible. The clock CK_o early-late information (X and Y) together with the two multi-phase clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, is provided to the ϕ -picker.

The idea behind the phase picking algorithm is depicted with the aid of eye diagrams in Fig. 3. When there is no phase difference between the consecutive packets, $\Delta\varphi = 0$ rad, either of the clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, will correctly sample the data bits of the phase shifted $(k+1)^{\text{th}}$ packet [see Fig. 3(a)]. This is also true for an antiphase step $\Delta\varphi = \pm\pi$ rad—not shown as this is a modulo- π process. For a phase step $-\pi < \Delta\varphi < 0$ rad, clock $CK_{+\pi/2}$ will sample the bits on or close to the transitions of the data eye, whereas clock $CK_{-\pi/2}$ will correctly sample the data [see Fig. 3(b)]. Similarly for a phase step $0 < \Delta\varphi < +\pi$ rad, clock $CK_{-\pi/2}$ will sample the bits on or close to the transitions, whereas clock $CK_{+\pi/2}$ will correctly sample the data [see Fig. 3(c)].

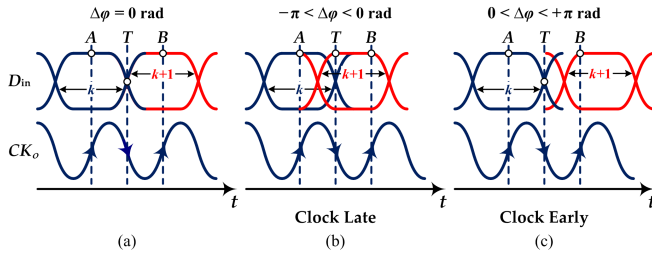


Fig. 2. (a) Three-point sampling scheme; (b) and (c) early-late waveforms.

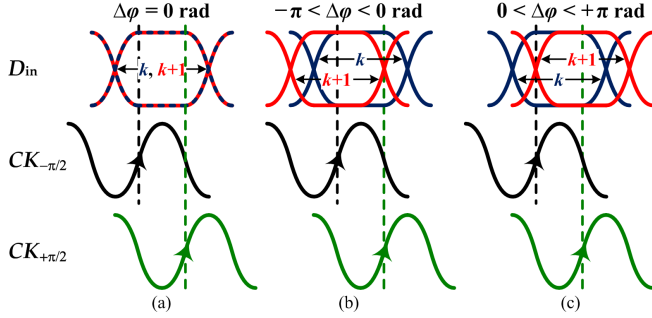


Fig. 3. CPA phase picking algorithm.

That is, regardless of any phase step, there will be at least one clock, either $CK_{-\pi/2}$ or $CK_{+\pi/2}$, that will yield an accurate sample. The ϕ -picker then selects the most accurate clock CK_{out} , from these two possibilities for driving the D-FF to retine the data; that is, sample the noisy data, yielding an output D_{out} with less jitter.

III. EXPERIMENTAL RESULTS

The BM-CDR is built from commercially available low cost/complexity electronics rated at 13 Gb/s. Specifically, the CDR is from Centellax (Part #TR1C1-A) and the CPA is built by integrating evaluations boards from Hittite Microwave: ϕ -shifters (Part #HMC538LP4), Alexander PD (Part #HMC6032LC4B), ϕ -picker comprised of an AND gate (Part #HMC672LC3C) and a 2:1 selector (Part #HMC748LC3C), and D-FF (Part #HMC673LC3C).

The BM-CDR is tested using a standard burst-mode test setup [2]. Fig. 4 shows the experimental BER performance of the CDR and BM-CDR at 10 Gb/s as a function of the phase step between two consecutive data bits, for a zero preamble length. As expected the worst-case phase steps for the CDR are around ± 50 ps ($\pm \pi$ rad) because these represent the half-bit periods, and therefore the CDR is sampling near the edges of the data eye, resulting in a loss of lock. At relatively small phase shifts (near 0 or 2π rad), we can easily achieve error-free operation, $BER < 10^{-11}$, because the CDR is almost sampling at the middle of each data bit. For the proposed BM-CDR, we achieve error-free operation for any phase step $|\Delta\phi| \leq 2\pi$ rad, allowing for instantaneous phase acquisition which can increase the effective throughput of the system by increasing the information rate, and also dramatically improve the physical efficiency of the upstream PON traffic to 99% for 32 ONUs [3]. The root-mean-square jitter of the recovered data is 2.5 ps as extracted from Fig. 5 which depicts the recovered data and clock in response to a $2^{15} - 1$ PRBS pattern.

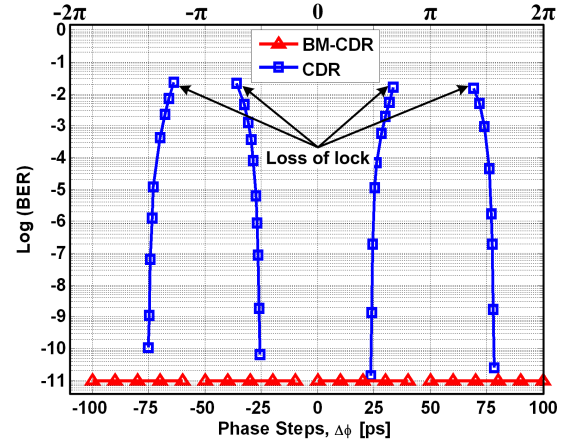


Fig. 4. BER performance of the CDR and BM-CDR (for zero preamble length) versus phase step.

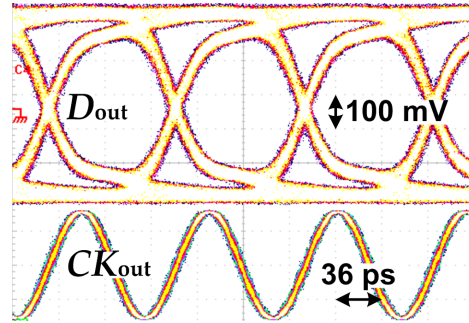


Fig. 5. Recovered data and clock.

IV. CONCLUSION

Recently, BM-CDRs that achieve instantaneous phase acquisition have been demonstrated for multi-access networks [3], [4]. These BM-CDRs are based on time oversampling techniques requiring electronics operating at twice or thrice the aggregate bit rate resulting in wasted power. They also have the knowledge of a predefined unique delimiter (start of packet) that they exploit as a signature for the phase picking algorithm. In contrast, our work based on space sampling, uses electronics operated at the bit rate with *no a priori* knowledge of the delimiter, leading to more efficient power consumption and being truly modular across application testbeds, respectively. Our eloquent, cost-effective, and scalable solution leverages the design of low-complexity commercial electronics.

REFERENCES

- [1] J. D. H. Alexander, "Clock recovery from random binary data," *Electron. Lett.*, vol. 11, no. 22, pp. 541–542, Oct. 1975.
- [2] A. Li, J. Faucher, and D. V. Plant, "Burst-mode clock and data recovery in optical multiaccess networks using broad-band PLLs," *IEEE Photon. Technol. Lett.*, vol. 18, no. 1, pp. 73–75, Jan. 2006.
- [3] B. J. Shastri and D. V. Plant, "5/10-Gb/s burst-mode clock and data recovery based on semiblind oversampling for PONs: theoretical and experimental," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 5, pp. 1298–1320, Sept.-Oct. 2010.
- [4] B. J. Shastri, Y.-B. M'Sallem, N. Zicha, L. A. Rusch, S. LaRochelle, and D. V. Plant, "An experimental study of burst-mode reception in a 1300-km deployed fiber link," *J. Opt. Commun. and Netw.*, vol. 2, no. 1, pp. 1–9, Jan. 2010.