A 20-GSample/s (10 GHz × 2 clocks) Burst-Mode CDR Based on Injection-Locking and Space Sampling for Access Networks

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Abstract: We demonstrate a novel 20-GSample/s burst-mode CDR circuit featuring instantaneous (0-bit) phase acquisition with BER<10^{-10} for any phase step (±2π rad) between successive bursts. Our design incorporates injection-locking and space sampling for clock phase recovery/alignment.

1. Introduction

As the explosive growth in Internet traffic continues, the need for highly-specialized low-cost integrated circuits is undeniable, with clock and data recovery (CDR) being a critical function in back plane routing and chip-to-chip interconnects. Furthermore, the traffic received on these multiaccess links—passive optical networks [1] and packet-switched networks [2]—is inherently bursty with asynchronous phase steps $|\Delta\varphi| \leq 2\pi$ rad, that exist between the consecutive k^{th} and $(k+1)^{th}$ packets. This inevitably causes conventional CDR circuits to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDR feedback loop enough time to settle down and thus acquire lock. However, the use of a preamble reduces the effective throughput and increases delay. Consequently, to deal with bursty data, these networks require a burst-mode CDR circuit (BM-CDR).

Recently, BM-CDRs that achieve instantaneous phase acquisition have been demonstrated [1][2]. These BM-CDRs are based on time oversampling which requires electronics operating at twice or thrice the aggregate bit rate resulting in wasted power. In addition, they exploit the knowledge of a predefined unique delimiter (start of packet) as a signature for phase picking.

In this paper, we present a novel BM-CDR architecture based on injection-locking technique and space sampling. The BM-CDR uses electronics operated *at* the bit rate with *no a priori* knowledge of the packet delimiter, leading to more efficient power consumption and making it truly modular across application testbeds, respectively. Our 20 GSample/s (10 GHz × 2 phase clocks) BM-CDR achieves a bit error rate (BER) < 10^{-10} with instantaneous (0-bit) phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad, between consecutive bits.

2. Proposed BM-CDR

A block diagram of the proposed BM-CDR is shown in Fig. 1. The BM-CDR is composed of a clock recovery circuit (CRC) and a clock phase aligner (CPA). The CRC is comprised of an edge-detector and a phase-locked loop (PLL) based voltage-controlled oscillator (VCO). It senses data D_{in}, and generates a synchronized clock CK. The input D_{in}, and its delayed replica are XORed to create pulses D'_{in}. These pulses indicate data transitions and also create spectral lines at the data rate and its harmonics. As a result, the VCO can easily injection-lock to the data rate [3]. Maintaining a half bit period between the two inputs of the XOR gate yields the strongest injection.

Burst-mode functionality is obtained with the space sampling CPA which utilizes multiphase clocks and a phase picking algorithm [4] based on an "early-late" detection principle. First, the ϕ-shifters provide multiple clocks: CK_o, $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases: 0, $-\pi/2$, and $+\pi/2$ rad, respectively, with respect to the clock CK, recovered by the CRC. Next, an Alexander PD [5] which inherently exhibits *bang-bang* (binary) characteristics is used to strobe the data waveform D_{in}, with consecutive clock CK_o edges, at multiple points. Depending on the phase difference between the consecutive packets, the PD can determine the location of the clock edge with respect to the data edge as follows: (a) if CK_o is late—lags D_{in}—when $-\pi < \Delta\varphi < 0$ rad, then $X\downarrow$ and $Y\uparrow$; (b) if CK_o is early—leads D_{in}—when $0 < \Delta\varphi < +\pi$ rad, then $X\uparrow$ and $Y\downarrow$; (c) if no data transition is present due to consecutive identical digits, then $X\downarrow$ and $Y\downarrow$; and (d) if no decision is possible, then $X\uparrow$ and $Y\uparrow$. The X and Y samples together with the clocks $CK_{-\pi/2}$ or $CK_{+\pi/2}$ are then provided to the phase picker. The phase picker combinational logic, comprised of an AND gate and a 2:1 selector, then selects the most accurate clock CK_{out}, from these two possibilities for driving the D flip-flop (D-FF). The D-FF retimes the data; that is, it samples the noisy data, yielding an output D_{out} with less jitter. Since the preceding process happens on a bit-by-bit basis, the result is instantaneous phase acquisition. This will be demonstrated next.

The BM-CDR is built from commercially available low cost/complexity electronics rated at 13 Gb/s. This is done by integrating evaluation boards from Hittite Microwave: XOR gate (HMC721LC3C), ϕ-shifters (HMC538LP4), Alexander PD (HMC6032LC4B), AND gate (HMC722LC3C), a 2:1 selector (HMC678LC3C), and D-FF (HMC673LC3C). The BM-CDR is tested using a standard burst-mode test setup [6].

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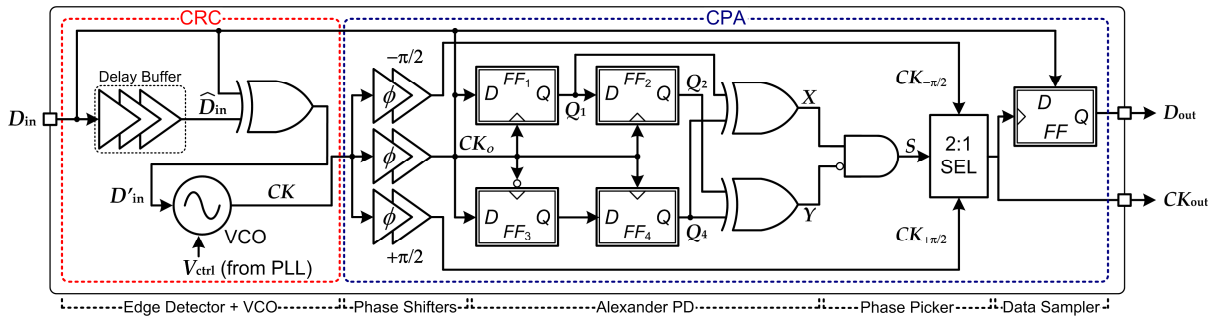
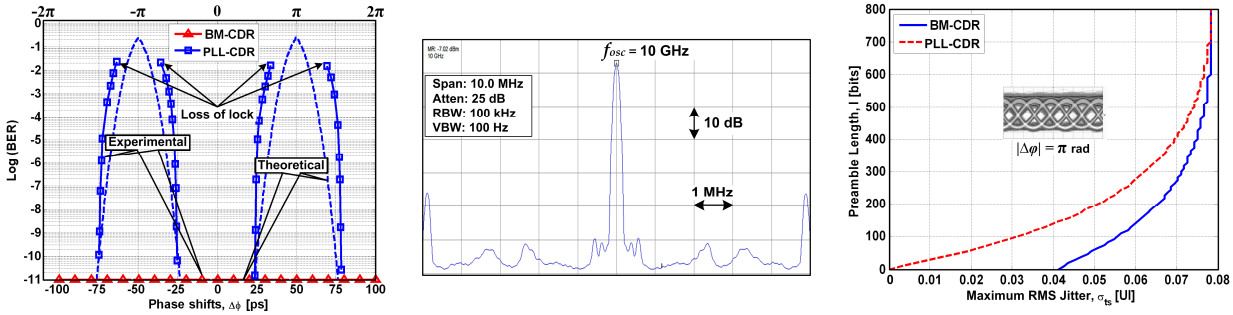


Fig. 1. Block diagram of the proposed BM-CDR.



(a) (b) (c)

Fig. 2. (a) BER performance of the BM-CDR (compared to a conventional PLL-based CDR) versus phase step for zero preamble length. (b) Recovered clock spectrum. (c). Preamble length versus rms jitter to achieve BER < 10^{-10}.

3. Results and Discussion

Fig. 2(a) shows the experimental BER performance of the BM-CDR compared to a conventional PLL-based CDR at 10 Gb/s as a function of the phase step between two consecutive data bits, for a zero preamble length. As expected, the worst-case phase steps for the CDR are around ±50 ps (±π rad) because these represent the half-bit periods, and therefore the CDR is sampling near the edges of the data eye, resulting in a loss of lock. At relatively small phase shifts (near 0 or 2π rad), we can easily achieve error-free operation, BER < 10^{-10}, because the CDR is almost sampling at the middle of each data bit. For the proposed BM-CDR, we achieve error-free operation for any phase step $|\Delta\varphi| \leq 2\pi$ rad, allowing for instantaneous phase acquisition. The experimental results are also in close agreement with the theoretical predictions in [1]. For the CDR, the theoretical bound is optimistic for BER > 10^{-6} as the probabilistic model accounts for the jitter input to the receiver and not for jitter generated by the circuitry; for example, VCO phase noise.

The output spectrum of the recovered clock is shown in Fig. 2(b). The phase noise at 100, 500, and 1000 kHz offset is approximately −24, −62, and −68 dBc/Hz, respectively. Fig. 2(c) shows the number of preamble bits l, required by the BM-CDR and CDR to obtain a BER ≤ 10^{-10} as a function of maximum allowable root mean square (rms) jitter for the worst case phase step $|\Delta\varphi| = \pi$ rad. The proposed BM-CDR is able to achieve instantaneous phase acquisition ($l = 0$) when the rms jitter $\sigma_{ts} \leq 0.04$ UI; this is true for any phase step $|\Delta\varphi| \leq 2\pi$ rad. However, it is not feasible for the CDR to achieve instantaneous phase acquisition as a jitter-free signal $\sigma_{ts}^{\max} = 0$ UI, is practically impossible.

4. Conclusion

We have demonstrated a novel BM-CDR architecture based on injection-locking technique and space sampling that achieves instantaneous phase acquisition. This can be used to increase the network's power budget by reducing the burst-mode sensitivity penalty or effective throughput by increasing the information rate. Our eloquent, scalable architecture leverages the design of low complexity commercial electronics, providing a cost-effective solution.

References

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