CMOS Compatible Add-drop Silicon-Organic Hybrid Racetrack Modulator

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***Abstract*— Optical modulators are vital in various applications, including data transmission, optical computing, and sensing. Current optical modulators rely on silicon due to compatibility with complementary metal-oxide semiconductor (CMOS). However, silicon modulators face challenges in terms of speed, energy efficiency, and area. This necessitates adding new materials to silicon platforms. Here, we design and fabricate a CMOS-compatible add-drop silicon-organic-hybrid racetrack modulator. It promises a high modulation bandwidth(96GHz) and low energy consumption(0.16fJ/bit), enabling the next generation of optical computing and data transmission.**

Keywords—*silicon-organic hybrid, silicon photonics, electro-optic modulators, electro-optic organic.*

2024 Photonics North (PN) | 979-8-3503-6636-5/24/$31.00 ©2024 IEEE | DOI: 10.1109/PN62551.2024.10621821

I. INTRODUCTION

Optical modulators are a vital component in photonics integrated circuits (PICs) for various applications, including data transmission [1], optical computing [2], and sensing [3]. Several metrics assess modulator performance: modulation speed, energy consumption, insertion loss (IL), footprint, and fabrication feasibility. Silicon photonics technology is now commercially available owing to their compatibility with Complementary Metal-Oxide Semiconductor (CMOS), enabling low-cost, high-volume production, reliable long-term performance, and large-scale integration of photonic components. The absence of second-order and a low third-order nonlinearity in silicon compels silicon modulators to rely on the free carrier dispersion (PN junction) for high-speed modulation. The speed and energy efficiency of silicon PN junction modulators are limited to 50 GHz and 70 fJ/bit [4]. To enhance speed and modulation efficiency, integrating highly nonlinear materials with silicon is crucial, leveraging large-scale silicon photonic integration. Cost-effective organic materials with high second-order nonlinearity, low power, exceptional electro-optic (EO) coefficients, and easy fabrication stand out among emerging materials [4]. Here, we design and fabricate an add-drop silicon-organic hybrid (SOH) partially-slotted racetrack modulator suggesting high-speed and low-drive voltage, power consumption, and IL. We employ Ansys/Lumerical for modeling and leverage commercial silicon photonics foundries for fabrication, followed by post-process deposition of organic material. To our knowledge, this is the first experimentally demonstrated add-drop slotted waveguide resonator-based SOH modulator with CMOS compatibility. Add-drop resonator-based modulators are necessary for WDM photonic transceivers, as well as vector-matrix multiplication in optical computing applications that require positive and negative weights.

II. DEVICE DESIGN AND FABRICATION

Fig. 1 depicts the studied add-drop SOH partially slotted racetrack modulator scheme, along with SEM images of the fabricated device. The dimensions include the racetrack radius ($r = 20\ \mu m$), coupling gap ($g = 140\ nm$), coupling length ($l = 10\ \mu m$), strip to slotted waveguide mode convertor length ($d = 12\ \mu m$), slotted waveguide length ($S_l = 12\ \mu m$), slab thickness ($t_2 = 90\ nm$), rib waveguide thickness ($t_1 = 220\ nm$), slotted waveguide rail width ($w_s = 240\ nm$), slot width ($a = 140\ nm$), and non-slotted waveguide width ($w = 0.5\ \mu m$). Partially slotted SOH racetrack modulator offers a smaller footprint and reduced loss compared to fully slotted MRMs by replacing the non-slotted bent waveguide with a lossy bent slotted waveguide [5]. The EO organic material, JRD1, with a strong EO coefficient ($n^3 r_{33}$=3850 pm/v) and glass transition $T_g = 82$ºC [6], is spin-coated in the post-processing step. The high EO coefficient leads to highly efficient modulation. The racetrack modulator was designed and simulated using Ansys/Lumerical photonics-electronics co-simulation platforms through our developed SOH modulators modeling methodology [7]. It was implemented in a multi-project wafer (MPW) run at a commercial silicon photonics foundry on a silicon-on-insulator (SOI) platform, utilizing 248 nm deep UV lithography.

III. RESULTS AND DISCUSSION

Fig. 2 illustrates the optical transmission spectrum ranging from 1516 nm to 1565 nm of the add-drop SOH racetrack modulator, featuring a 2.6 nm free spectral range (FSR), extinction ratios (ER) of 13 dB and 6 dB, -3db linewidths of 0.74 nm and 1.1 nm, quality factors (Q) of 2000 and 1400 for the through and drop ports, respectively. The device has an insertion loss (IL) of 2.2 dB. Device optimization through additional simulations shows a higher coupling coefficient realizes an identical drop and through port spectrums. Using our precise SOH modulators modeling methodology [7], we achieved $V_\pi = 0.35\ V$, $R = 250\ \Omega$ (resistance), and $C = 5fF$ (capacitance) for the proposed SOH racetrack modulator, resulting in an energy per bit of 0.16 fJ/bit. The resistance of 220 Ω was experimentally measured, aligning with simulations. The modulation bandwidth, constrained by either optical bandwidth ($BW_{opt} = {}^{w_0}/_{2\pi Q}$) or electrical bandwidth ($BW_{elec} = {}^{1}/_{2\pi RC}$), calculated at 96 GHz (constrained by BW_{opt}). Fabrication rules with a 90 nm slab contribute to high-slotted waveguide loss, limiting footprint, Q-factor, and ER. Reducing slab thickness, which is available in some silicon photonics foundries, further eases device design trade-offs. It also allows fabricating a 2-side partially slotted racetrack modulator, offering higher modulation efficiency and lower energy consumption.

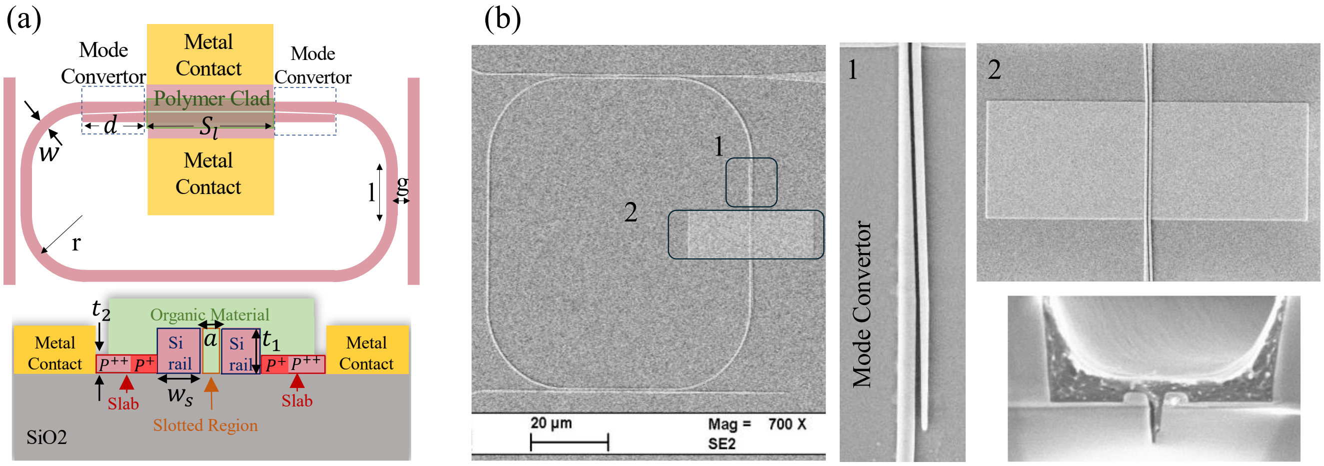

Fig. 1 Schematic (a) and SEM image (b) of the proposed add-drop SOH partially-slotted racetrack modulator, showcasing both top and cross-sectional views.

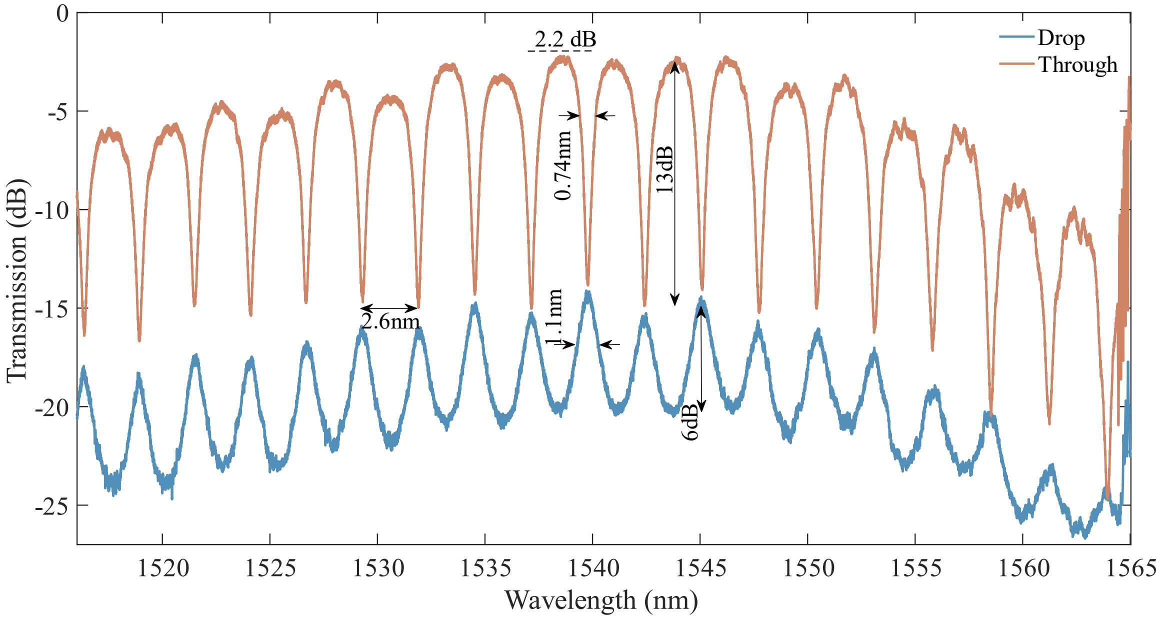

Fig. 2 The optical transmission profiles of the SOH add-drop partially slotted racetrack modulator showing $FSR = 2.6\ nm, IL = 2.2\ dB, ER = 13\ dB\ (6\ dB), -3\ dB\ linewidth = 0.74\ nm\ (1.1\ nm)$ for the through (drop) ports.

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