Emerging Photonic Hardware Platforms

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Abstract: Photonic integrated circuit technology could revolutionize optical information processing, beyond conventional binary-logic approaches, granting the capacity of ultrafast-categorization and decision-making. We will discuss the progress and requirements of scalable and reconfigurable emerging photonic hardware platforms.

OCIS codes: (200.0200) Optics in computing; (200.3050) Information processing; (200.4650) Optical interconnects; (250.0250) Optoelectronics; (250.5300) Photonic integrated circuits; (250.5960) Semiconductor lasers.

Photonics has revolutionized information communication, while electronics, in parallel, has dominated information processing. Recently, there has been a determined exploration of the unifying boundaries between photonics and electronics on the same substrate, driven in part as Moore's Law approaches its long-anticipated end [1, 2]. For example, the computational efficiency (multiply-accumulate (MAC) operations per joule) for digital processing has leveled-off around 100 pJ per MAC [2]. As a result, there has been a widening gap between computational efficiency and the next generation needs, such as Big Data applications which require advanced pattern matching and analysis on increasingly dense, voluminous data in real-time. This in turn, has led to expeditious advances in: (1) emerging devices that are called beyond-CMOS or More-than-Moore, (2) novel processing or unconventional computing architectures called beyond-von Neumann, that are bio-inspired i.e. *neuromorphic*, and (3) CMOS-compatible photonic interconnect technologies. Collectively, these research endeavors have opened opportunities for emerging photonic hardware platforms that are reconfigurable i.e. *programmable optical integrated circuits* (POIC) such as *photonic spike processors* [3–8]. Such chips in the near future could combine ultrafast operation, moderate complexity, and full programmability, extending the bounds of computing for applications such as navigation control on hypersonic aircrafts, and real-time sensing and analysis of the radio frequency (RF) spectrum. We will discuss the current progress and requirements of such a platform.

In a photonic spike processor, information is encoded as *events* in the temporal and spatial domain of spikes (or optical pulses). This hybrid coding scheme is digital in amplitude but analog in time and benefits from the bandwidth efficiency of analog processing and the robustness to noise of digital communication. Optical pulses are received, processed, and generated by certain class of semiconductor devices that exhibit *excitability*—a nonlinear dynamical mechanism underlying all-or-none responses to small perturbations [9]. Optoelectronic devices operating in the excitable regime are dynamically analogous with the spiking dynamics observed in *neuron biophysics* but roughly eight orders of magnitude faster. Example of *excitable* photonic devices include two-section gain and saturable absorber (SA) lasers [3, 6, 10], semiconductor ring [11–13] and microdisk lasers [14, 15], two-dimensional photonic crystal nanocavities [16, 17], resonant tunneling diode photodetector and laser diode [7], semiconductor lasers based on optical injection [18–20] and optical feedback [21–24], and polarization switching in VCSELs [8].

Using a gain and SA excitable laser, we recently demonstrated [3] the first unified, experimental demonstration of low-level spike processing functions in an optical platform. Excitatory input pulses to this laser increase the carrier concentration within the gain region by an amount proportional to its energy through gain enhancement. Beyond some excitation energy, the absorber is saturated, resulting in the release of a pulse. This is followed by a relative *refractory period* during which the arrival of a second excitatory pulse is unable to cause the laser to fire as the gain recovers. We showed that this platform can simultaneously exhibit logic-level restoration, cascadability and input-output isolation—fundamental challenges in optical information processing [25–27]. We also implemented the classic spike processing tasks of temporal pattern detection and stable recurrent memory—while simple, these fundamental behaviors underly higher level processing. We will review the recent surge of interest in the information processing abilities of such excitable optoelectronic devices.

The field is now reaching a critical juncture where there is shift from studying single excitable (spiking) devices to studying an interconnected network of such devices to build a photonic spike processor. We recently proposed [4]

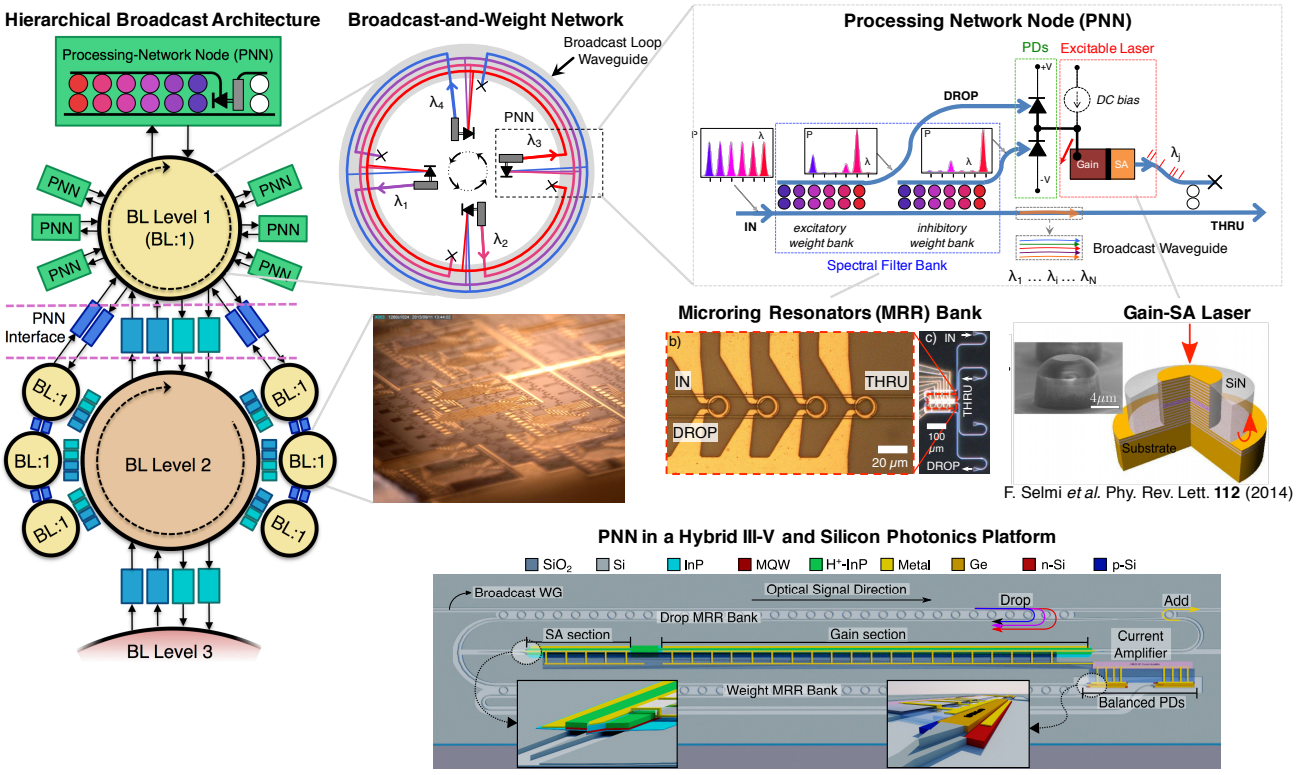

Fig. 1. Concepts, devices, and networks to build a photonic spike processor including gain-SA excitable lasers, MRR weight banks, PNNs, broadcast-and-weight networks. Also shown is a three-dimensional sketch of a PNN in a hybrid III-V and silicon platform.

an on-chip networking architecture called *broadcast-and-weight* (Fig. 1) that could support massively parallel (all-to-all) interconnection between excitable lasers. It has similarities with the fiber networking technique broadcast-and-select, which channelizes usable bandwidth using wavelength division multiplexing (WDM); however, the protocol flattens the traditional layered hierarchy of optical networks, accomplishing physical, logical, and processing tasks in a compact computational primitive. Although the processing circuits are unconventional, the required device set is compatible with mainstream PIC platforms in silicon, which make heavy use of WDM techniques.

Within this network, an interface called *processing network node* (PNN) (Fig. 1), gives the ability for one laser to communicate with others. A PNN handles inputs from multiple sources by weighting and spatially summing (i.e. weighted addition), before sending the resulting signal to an excitable laser. The front-end of the PNN consists of two spectral filter banks of continuously tunable microring resonator (MRR) weight banks that partially drop WDM channels that are present *without* demultiplexing. The use of MRRs as continuous-valued weights has recently been shown [28,29]. One filter bank represents the weights of excitatory (positive) input connections while the other controls inhibitory (negative) inputs. These weight profiles could be stored in local co-integrated or off-chip CMOS memory. Balanced photodetectors output a current that represents total optical power, thus computing the weighted sum of WDM inputs in the process of transducing them to an electronic signal, which is capable of modulating an excitable laser. In this way, each such PNN is connected with every other PNN in a *broadcast loop* using a broadcast-and-weight network. That is, the broadcast loop is fully multiplexed and capable of supporting N^2 interconnects in just one transparent link (waveguide) with N WDM channels; an electronic interconnect would require, at best, $N(N-1)/2$ links to achieve the same non-blocking behavior. Recent channel density studies [30] quantified analysis for multiwavelength analog networks, and derived a limit of 108 PNNs per broadcast loop, of which many can co-exist on a single chip.

An integrated hardware platform has been proposed [10] to be built on a hybrid III-V and silicon photonics platform (Fig. 1). III-V compound semiconductor technology, such as indium phosphide (InP) and gallium arsenide (GaAs), is at the forefront of providing *active* elements like lasers, amplifiers and detectors. Silicon, in parallel, brings compatibility with CMOS fabrication processes and low-loss *passive* components like waveguides and resonators. Scalable and fully reconfigurable networks of excitable lasers can be implemented in the silicon photonic layer of modern hybrid

integration platforms, in which spiking lasers in a bonded InP layer are densely interconnected through a silicon layer. Such a photonic spike processor will potentially be able to support several thousand interconnected photonic spike primitives (PNNs). It is predicted [31] that such a chip would have a computational efficiency of 260 fJ per MAC, which surpasses the energy efficiency wall by two orders of magnitude while operating at very high speeds (i.e. signal bandwidths 10 GHz).

The emerging field of photonic spike processors has received tremendous interest and continues to receive further developments as PICs increase in performance and scale. As novel applications requiring real-time, ultrafast processing—such as the exploitation of the RF spectrum—become more critical, we expect that these systems will find use in a variety of high performance, time-critical environments.

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