3.5 Gb/s Burst-Mode Clock Phase Aligner for Gigabit Passive Optical Networks

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***Abstract*— We demonstrate a 3.5 Gb/s burst-mode receiver featuring instantaneous (0-bit) phase acquisition for any phase (±2π) between packets in GPON. Our design is based on a 2× oversampling local oscillator and a phase picking algorithm.**

I. Introduction

Passive optical networks (PONs) are an emerging multi-access network technology that provides a low-cost method of deploying fiber-to-the-home. Fig. 1 shows an example of a PON. In the upstream direction, the network is point-to-multipoint: using time-division multiple access (TDMA), multiple optical network units (ONUs) transmit bursty data to the optical line terminal (OLT). Due to optical path differences, packets can vary in phase and amplitude when received by the OLT. To deal with these variations, the OLT requires a burstmode receiver (BMRx). The BMRx front-end is responsible for amplitude recovery, whereas clock and data recovery (CDR) is performed with phase acquisition by a clock phase aligner (CPA). This paper focuses on the CPA aspect of the BMRx.

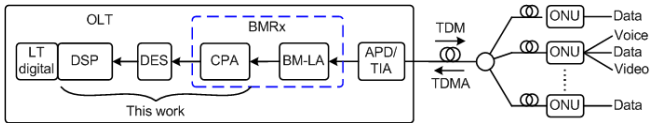

Fig. 1: A Generic PON showing our work in context (APD: avalanche photodiode; TIA: transimpedance amplifier; BM-LA; burst-mode limiting amplifier; Des: deserializer; DSP: digital signal processing).

The most important characteristic of the BM-CPA is its phase acquisition time which must be as short as possible. In [1], the authors proposed a BM-CPA at 622 Mb/s by making use of an oversampling CDR operated at twice the bit rate, and a phase picking algorithm. In this paper, we demonstrate a 3.5 Gb/s BM-CPA that achieves instantaneous (0-bit) phase acquisition for any phase step (±2π) between consecutive packets, with packet loss ratio (PLR) < 10^{-6} and bit-error rate (BER) < 10^{-10}. In addition, we achieve this in a much more cost-effective manner by employing a simple local oscillator (LO), and thus eliminating the need of complex and expensive CDR circuits based on phase-locked loops (PLLs).

II. Burst-Mode Clock Phase Aligner

A block diagram of the BM-CPA is shown in Fig. 2. An LO or a CDR can be used to either generate a clock signal, or recover the clock from the incoming bursty data, respectively. The CDR/LO is followed by a 1:16 deserializer from Maxim-IC (MAX3995). The parallel data and the divided clock are then brought onto a Virtex IV FPGA from Xilinx for further processing. The challenge in designing a gigabit-capable receiver based on FPGAs, is of limited processing speed of digital logic on commercially available FPGAs. Thus, the proposed BM-CPA has an integrated double data rate (DDR) 1:8 deserializer, programmed on the FPGA, to further parallelize the data and the clock to a frequency that can be processed by the digital logic. The CPA can be turned on or by-passed to operate at different modes for experimental purposes.

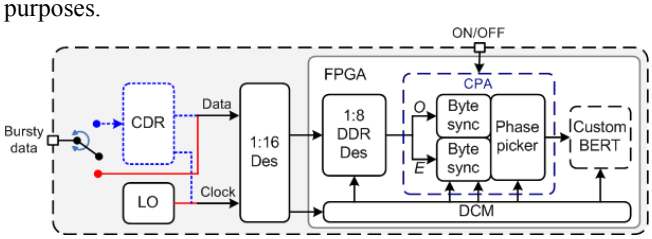

Fig. 2: Block diagram of BM-CPA (DCM: digital clock manager.)

The idea behind the CPA is based on a simple, fast, and effective algorithm. The odd and the even samples resulting from sampling the data twice on the alternate (odd and even) clock rising edges, are forwarded to path *O* and to path *E*, respectively. The two byte synchronizers attempt to detect the delimiter on either the odd and/or even samples of the data respectively. Since the clock rate is twice the data rate, there is always at least one clock (odd or even) edge that samples the data correctly, regardless of the phase step. Thus, the phase picker can use feedback from the byte synchronizers to select the right path. The realigned data is then sent to the FPGA based BERT, implemented to selectively perform BER and PLR measurements on the payload of the packets.

In essence, the BM-CPA supports three modes of operation: 1) conventional mode − essentially a SONET CDR, 2) burst-mode with CDR − CPA turned on with CDR locking at twice the data rate, 3) burst-mode with LO − CPA turned on with LO locking at twice the data rate. These modes of operation are useful in measuring the relative performances.

III. Results and Discussion

Fig. 3 shows the experimental setup to measure the phase acquisition time of the BM-CPA in the three modes of operation. Bursty upstream PON traffic is generated by adjusting the phase $|\Delta\varphi| \leq 2\pi$ rads on a 1-ps resolution, between alternating packets from two programmable ports of a pattern generator, which are then concatenated via a power combiner (PC). These packets are formed from guard bits, preamble bits, delimiter bits, 2^{15}-1 PRBS payload bits, and

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comma bits.

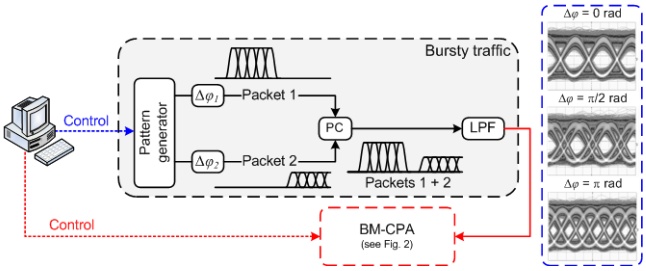

Fig. 3: Experimental setup (LPF: low-pass filter).

Fig. 4 shows the PLR performance of the system as a function of the phase difference between consecutive packets. Fig. 4(a) depicts the phase step response of the receiver with only the CDR and the CPA turned off (mode 1), for different preamble lengths at 1.25 Gb/s. The reason why we have a bell-shaped curve centered at 400 ps is that this is the half bit period corresponding to the worst-case phase step (π rads), and therefore the CDR is sampling exactly at the edge of the eye diagram. Preamble bits ("1010..." pattern) can be inserted at the beginning of the packets to help the CDR settle down and acquire lock. However, the use of the preamble reduces effective throughput and increases delay. As the preamble length is increased, there is an improvement in the PLR. We observe error-free operation (PLR < 10^{-6}) for any phase step after 28 preamble bits. This does not satisfy the 28-bit requirement for both, phase and amplitude recovery, specified in the G.984.2 standard [2].

However, by switching on the burst-mode functionality of the receiver with the CPA (mode 2) as shown in Fig. 4 (b), we observe error-free operation for any phase step ($0 \le \Delta\varphi \le 2\pi$ rads) with *no* preamble bits, allowing for instantaneous phase acquisition − well below the 28-bit specification. We also plot the phase step response of the receiver at 2.5 Gb/s[1]. Again, as expected, with only the CDR, the curve is centered at 200 ps as this is the half bit period corresponding to the worst-case phase step (π rads) at 2.5 Gb/s.

By replacing the PLL based CDR by the LO (mode 3), we also obtain error-free operation for any phase step with no preamble bits for data rates up to 3.5 Gb/s as demonstrated in Fig. 4(c). To the best of our knowledge, this is the first time that a BM-CPA is successfully implemented without CDR circuitry. This novel design is simpler and cheaper, without any reduction in performance.

IV. Conclusion

In conclusion, we successfully implemented a BM-CPA that operates up to 3.5 Gb/s and provides instantaneous phase acquisition. The price to pay is faster electronics. However, our CDR-free BM-CPA greatly reduces the complexity of electronics, providing a cost-effective solution for GPON receivers. We note that a sensitivity penalty results from the quick extraction of the decision threshold and clock phase from a short preamble at the start of each packet [3]. However, by reducing the phase acquisition time, as demonstrated in this work, more bits are left for amplitude recovery, thus reducing the burst-mode sensitivity penalty. Alternatively, with the reduced number of preamble bits, more bits can be used for the payload, thereby increasing the information rate.

[1] The CDR could not be tested for different preamble lengths at 3.5 Gb/s as this rate is not supported on commercially available SONET CDRs.

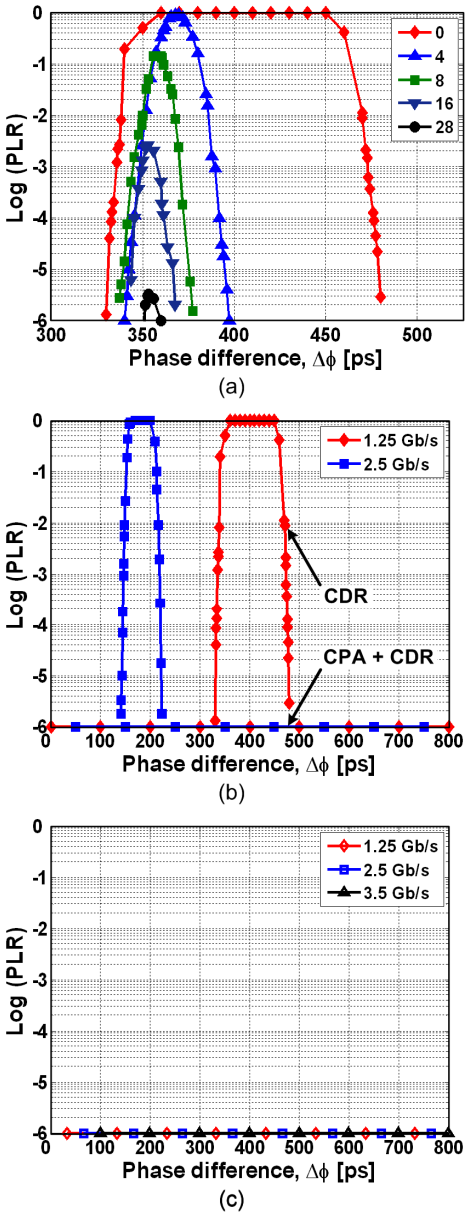

Fig. 4: PLR performance for the BM-CPA.

Acknowledgement

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[2] *Gigabit-capable Passive Optical Networks: Physical Media Dependent layer specification*, ITU-T Recommendation G.984.2., 2003.

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