The Silicon-Based XOI Wafer: The Most General Electronics-Photonics Platform for Computing, Sensing, and Communications

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***Abstract*—This paper proposes that the 300-mm-diameter silicon wafer coated with a thin insulator layer, which becomes a buried layer, is the most general and most capable platform for high-volume foundry-manufactured, waveguided, photonic integrated circuits (PICs) and for the on-wafer electronics that control and signal-process the photonics. We call this "on insulator" platform an electronic- photonic (or optoelectronic) integrated-circuit wafer. For a few potential applications like "general intelligence" (Shainline et al., 2021), entire wafers would be deployed. However, in almost every case, the wafer will be diced into hundreds of electronic-photonic chips (chips are the real aim of wafer creation). Those chips would be commercial products or custom-made, application-specific PICs. The goal of this paper is to present a detailed vision of the ultimate electronic- photonic wafers that: (1) serve a vast range of applications, (2) operate at any wavelength within the ultraviolet, visible, near-infrared and middle infrared, (3) provide low-loss, well-confined optical waveguiding across the wafer, (4) utilize an optimized or application-specific combination of photonic materials including semiconductors, insulators, ferroelectrics, poled polymers (Xu et al., 2022), phase-change materials (PCMs) (Wuttig et al., 2017), plasmonics (Moor et al., 2021), (Amin et al., 2021), and 2D materials such as graphene (Liu et al., 2020), (5) offer one-or-more practical electro-optical modulation-and-switching mechanisms that are discussed below, (6) offer on-wafer laser diodes, wavelength-multiplexed comb sources, LEDs, optical amplifiers, and photodetectors, (7) provide a full range of CMOS-or-"other" control electronics as well as electronic memories and data converters (analog-to-digital and digital-to-analog), and (8) are manufacturable in volume by proven techniques such as wafer bonding, smart cut, and hetero-epitaxy– or are made by emerging methods. The insulator mentioned above could be silicon dioxide (SiO_2) or alumina (Al_2O_3), or silicon nitride (Si_3N_4 or SiN). SiO_2 is generally preferred, but the Al_2O_3 and the SiN offer better mid-infrared transparency than the oxide.**

***Index Terms*—Group-IV photonics, heterogeneous integration, optical computing, optoelectronic integration, quantum photonics, Silicon-on-insulator, wafer-scale integration.**

I. Real and Potential Applications

THE advantages and inherent benefits of the "on insulator" (OI) wafer are: high refractive-index contrast, high mode confinement, reduced leakage and field penetration, large-scale integration, wide-bandwidth operation, light manipulation flexibility, and integration compatibility.

The generalized wafer, by definition, has the broadest range of applications. The topic of this JSTQE Special Issue is optical computing, and it is clear to us that the Si-based electronic-photonic wafers apply strongly to neuromorphic and artificial intelligence (AI) analog computing [7], [8], electronic- photonic digital computing [9], reservoir computing [10], [11], Ising machines [12], [13], and optical memories [3], [14], [15]. There are additional wafer applications, some well-known and some arising. They include advanced coherent transceiver chips for terabit fiber-optic communications such as long-haul telecom and shorter-distance data-center interconnections with optoelectronic chips providing broadband *N x N* electro-optical (EO) in-rack circuit and ethernet switching. Chip-to-chip interconnects are also emerging. There are important sensing applications [16] in the areas of chemical (e.g., trace gas), biological (e.g., toxins detection), medical (e.g., blood glucose), and physical (e.g., gyroscopes for navigation) sensing. On-wafer spectrometers are the main sensing avenue. Other important applications include quantum computing [17], quantum metrology [18], quantum cryptography [17], microwave photonics [19], terahertz photonics [20], 5G and 6G wireless communications [21], underwater communications [22], and the Internet-Of-Things [23]. The OI approach gives the high-quality passive and active waveguided components needed in these applications and provides those components at all the desired wavelength bands.

Nonlinear optical (NLO) circuits are key applications. These include microcomb generation [24] and optical frequency translation, such as second- and third-harmonic generation and difference-frequency down-conversion [17], even into the terahertz region. A major NLO application is quantum-photonic sources such as entangled-photon pair generators, including three-wave mixing for spontaneous parametric down-conversion and spontaneous four-wave mixing [17]. NLO can also realize neuromorphic-related nonlinear activation devices [25], [26].

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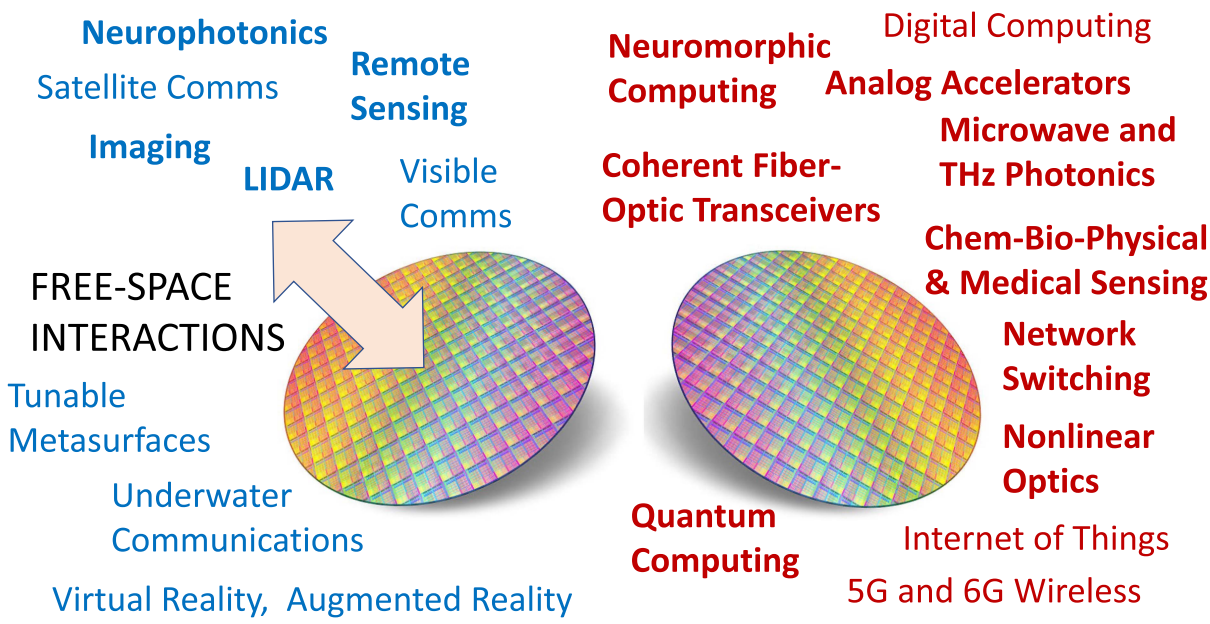

Fig. 1. XOIOE applications in two categories. Applications listed in bold type are at a higher stage of development than those shown in regular type.

The intensity-dependent refractive indices of semiconductors, the DC and AC Kerr refractive indices, are the basis of additional NLO applications [27]. NLO users of the general wafer can use the NLO response of bulk compound semiconductors or the nano-layered quantum-well and superlattice waveguides presented below.

The general wafer can transmit/radiate light into free space, and the wafer can easily receive light incident from free space. Consequently, these Si-based general wafers enable critical applications in LIDAR, imaging, satellite communications, virtual reality, augmented reality, *N x N* spatial light modulation, and tunable metasurfaces. These applications do not demand waveguiding, so the OI approach is not imperative. However, OI is often a performance booster in "spatial" apps. Another capability of the general wafer is in the composite "free-and-guided" category, where a microelectromechanical (MEMs) "system layer" forms the top layer of the wafer [28] to provide, for example, 3D imaging-LIDAR using *N x N* MEMs-actuated focal-plane-switched waveguide-grating-coupler antennas [29]. MEMs have proven very capable in *N x N* PIC switching. Fig. 1 summarizes the applications.

Although most applications are at 300K, we include 4K cryogenic wafer applications in this current roadmap because several key optical-computing opportunities become actualized at this low temperature. Those applications include quantum-photonic computing and neuromorphic photonic computing [1], [7]. Several kinds of specialized cryogenic electronic circuits can facilitate cryogenic photonics. The principal ones are superconducting 4K-Josephson-junction electronics and low-power III-V electronics for 4K, comprised of InP high electron mobility transistors (HEMTs) [30]. Several materials-combinations for 4K applications have been demonstrated, such as barium-titanate-on-Si electro-optical (EO) modulators and III-V laser diodes.

II. High-Contrast Low-Loss Waveguiding

The core of each PIC strip-or-rib waveguide has an upper cladding and a lower cladding. If the strip is grown or deposited upon an (uncoated) bulk-crystal substrate wafer, Si becomes the lower cladding. For many air/core/Si cases, the light will likely leak out into the substrate because the core semiconductor will have an index of refraction lower than the substrate's index. We propose the technique well-known for years in the SOI art to prevent this leakage. The method is to deposit an optically thick layer of SiO_2 (about 2 μm thick) upon the Si wafer, where the 1.45 index of the oxide is in every case lower than the core index. This "high contrast" of core/clad indices always happens and ensures the bunching of the optical mode in the core. In summary, the OI wafer is necessary and sufficient to provide excellent waveguides in all wafer cases. It is possible and desirable to utilize: (1) III-V and/or II-VI and/or group-IV semiconductors (and their alloys) such as InGaAsP, AlGaAs, InGaAs, AlGaN, and GeSn; (2) insulators such as SiN, Ta_2O_5, diamond, and silicon oxynitride,(3) ferroelectrics such as $LiNbO_3$, $KNbO_3$, and $BaTiO_3$, (4) organic polymers such as chromophores, (5) 2D materials like graphene, and (6) non-volatile PCMs like Sb_2Se_3. SiN does not exhibit electro-optical effects, so it is recommended here that passive SiNOI PICs should be hybrid-integrated with the active materials just listed. For wafers operating in the visible, photodetectors made of Si are just one of several good PD choices.

The industry-standard silicon photonics (SiPh) platform uses silicon-on-insulator (SOI), and we suggest going well beyond the SiPh materials repertoire of Si and Ge to attain expanded wavelengths-coverage as well as lasing and gain. Group IV photonics (GFP) is a widely expanded version of SiPh, and one embodiment of GFP deploys GeSn heterostructures. We project that the GeSn/SiGeSn heterostructures being developed

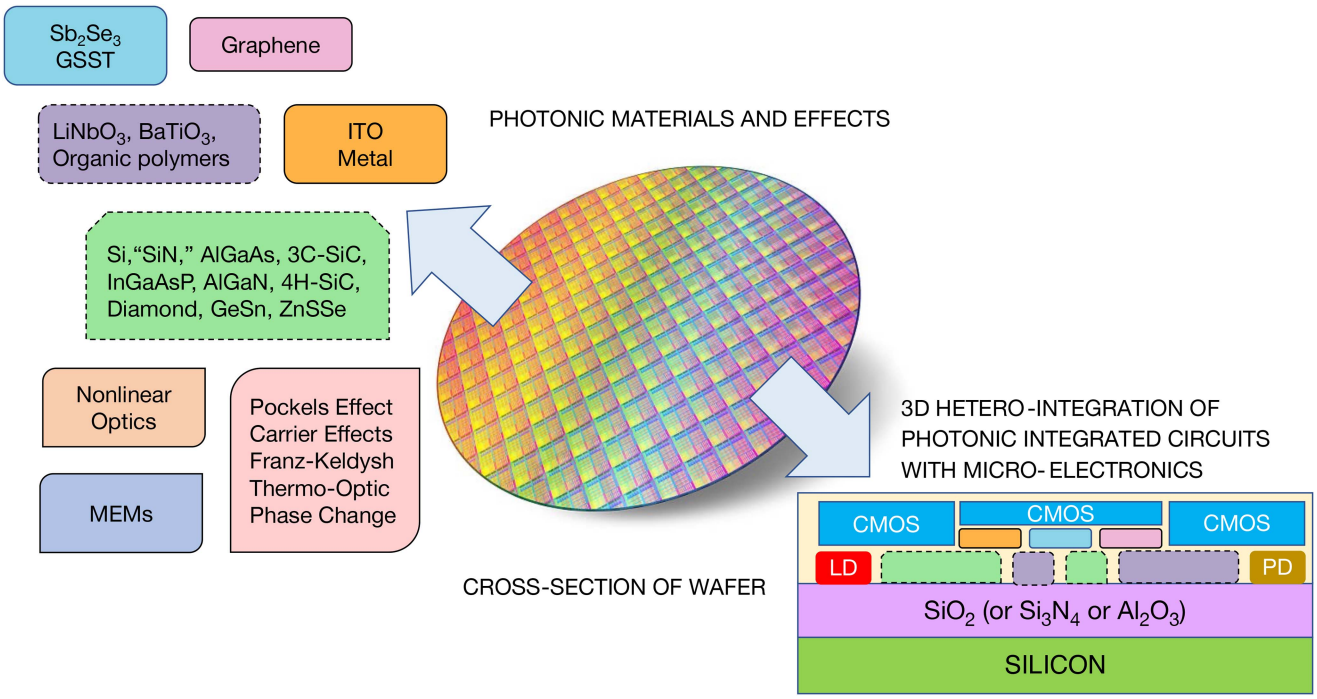

Fig. 2. XOIOE wafer materials and EO effects. The cross-section shows schematically the 3D-opto-electronic hetero-integration.

today will (in the not-so-distant future) yield room-temperature on-wafer laser diodes for operation at 2 to 4 μm wavelengths [31].

Also, high-performance GeSn on-wafer photodetectors are available today. Together these will form excellent monolithic GeSn PICs on the GeOI wafer foundation. Looking beyond GeSn, GFP generally employs CSiGeSn alloys. Therefore, GFP offers ultraviolet and visible-light application through diamond photonics and silicon-carbide photonics SiCOI [33], which are well respected in the present art. Fig. 2 summarizes the XOI materials and effects.

III. Wafer Terminology

The symbol "X" is used here to signify a specifically selected combination of OI photonic materials, and we are examining here the XOI possibilities. Silicon-based or III-V electronics will be linked to that X selection to control XOI and to analyze optical signals. These electronics and optics form an optoelectronic (OE) system. For that reason, we will introduce the new term XOIOE to refer to all the wafers proposed in this paper.

IV. Specific Xoioe Examples and Recommendations

Bonding two photonic wafers forms the on-insulator $LiNbO_3$ and $BaTiO_3$ platforms; for example, a $LiNbO_3$ handle wafer is bonded to SiO_2/Si. In the new-generation Lithium-Niobate on Insulator LNOI, the ion slicing method thins or refines the bonded first-wafer [34]. $BaTiO_3$ is often formed upon a lower-index $SrTiO_3$ layer that rests upon an insulator. According to [35], [36], wafer-bonding is employed to create $BaTiO_3$-on-SOI PICs labeled here as BTOI. An alternative to bonding is to deposit "large area" oriented BTO film on the SiO_2/Si and then deposit local Si or SiN rib waveguide elements on that film [37].

Focusing next on semiconductors for X, we first list (in parenthesis) the wavelength-of-operation above which the photonic material becomes transparent: GaAs (871 nm), AlAs (574 nm), InP (923 nm), GaP (549 nm), AlP (506 nm),ZnS (337 nm), ZnSe (439 nm), $LiNbO_3$ (340nm), $BaTiO_3$ (390 nm), SiO_2 (200 nm), amorphous silicon nitride (480 nm), diamond (226 nm), 3C-SiC (525 nm), 4H-SiC (384 nm), Si (1148 nm), Ge (1850 nm), z-GaN (388 nm), z-AlN (232 nm), w-GaN (366 nm), and w-AlN (194 nm), where z is zincblende and w is wurtzite. This indicates photonic device operation at 200 to 400-nm UV for a few of these and within the 400 to 700-nm visible band for several of these. Next, we detail some XOIOE specifics. The general idea is to deploy binary and ternary alloys of elemental or compound semiconductors.

The SiCOI platform is practical and worthy of receiving more attention. The cubic and hexagonal forms have proven feasible, and the literature presents direct wafer-bonding experiments for both structures [33], [38], where 3C-SiCOI and 4H-SiCOI were achieved. The fabrication methods for 4H are currently more advanced than for 3C [38]. Waveguided PICs are achievable in both 3C-SiCOI and 4H-SiCOI. A second important approach uses the SiC-to-AlN/GaN lattice match, a feature we recommend for the superlattices described below. In summary, the 3C and 4H SiCOI offer feasibility and practicality with wide bandgap, high optical nonlinearities, low-loss waveguiding, and CMOS-process compatibility.

The use of AlGaN on a sapphire wafer was discussed in [39], and here we present alternative versions of AlGaNOI.

As highlighted in [39], visible-light waveguides (as in AlGaN) demand high-resolution lithography for waveguide fabrication. The wafer-bonding approach to InPOI, as outlined in [40], is a bonding that also applies to the versatile InGaAsPOI alloys approach. Through selective InP epitaxy on bare oxide, InP has recently been successfully integrated on-insulator by creating sub-micron InP wires and InP lateral membranes using metal-organic chemical vapor deposition (MOCVD) [41]. Experimental results on AlGaAsOI are reported in [42], and we agree with their compound-semiconductor-on-insulator proposals and the 2022 roadmap [17], where the authors point out the key role of AlGaAsOI in quantum information processing enabled by nonlinearities and by monolithic on-wafer integration of III-V light sources including quantum dot sources. CMOS integration with AlGaAsOI is one of several electronics possibilities.

As mentioned, bonding is not needed for GeSn/SiGeSn functional layers because the starting wafer is either SOI or GeOI, meaning that low-strain GeSn heterolayers are grown directly upon thin GeSn buffer layers on SOI or GeOI, leading to functional monolithic GeSn/SiGeSn PICs labeled GeSn-OI. In addition to its role as a foundation for monolithic laser/modulator/detector GFP PICs, GeOI could provide a lattice-matched substrate for active III-V and II-VI "hetero" photonics. For example, AlGaAs/GeOI has a versatile PIC layer created without bonding. However, since the waveguide core will include Ge, the wavelength of operation will then be larger than 1850 nm. With that constraint, we could deploy XOIOE wafers of ZnSe/GeOI and AlGaAs/GeOI. The OI labels in this paragraph imply hetero-structured functional layers on the wafer: GaAs/AlGaAs, InP/InGaAs, AlN/AlGaN, and GeSn/Ge.

If photonics follows a path like that of microelectronics, there will always be a variety of integration strategies that balance performance and cost under different constraints. Co-integration approaches under active development and high-volume production include multichip modules (MCM), a.k.a. system-in-package (SiP), and system-on-chip (SoC). MCMs interface known-good dies originating from separately optimized processes, for example, logic and RAM stacking. A parallel of MCM would be photonic wire bonding [43]. SoCs integrate multiple subsystems monolithically, for example, memory caches on the CPU. SoCs virtually eliminate interfacial overhead and complex assembly steps while they tend to face greater fabrication complexity and compromises involved in optimizing multiple targets in a single process. A parallel of SoC would be photonics based on CMOS-adjacent processes [44]; however, the monolithic integration of light sources remains a major challenge because "monolithic" implies lattice-matched local-area epitaxy of QW layers on the waveguiding layer. XOIOE can be seen as an SoC approach with many possible incarnations.

V. Quantum-Well-on-Insulator NLO Circuits

In the category of electrically injected light sources, it is clear that quantum dots (QDs) and quantum wells (QWs) contribute strongly to the present experimental on-insulator wafers; for example, the InGaAs QD quantum source on 4H SiC [45] and the InGaAs LDs on Si [46]. In addition, there is a second category of QW photonics that employs passive QW waveguides with a multi-layered core, waveguides designed for very large NLO response to optical pumping. We shall now examine the multiple-QW PICs denoted here as QWOI (where waveguide layers are less than 20 nm thick) and propose a second group of thin-layer superlattice SLOI waveguides. Generally, the QWs and SLs offer enhanced three-wave mixing and four-wave mixing. For the three-wave SLOI case, there is also an active device available: the electroded waveguide for which a large Pockels effect has been engineered.

For QWOI, we have a new design [47] in which the multiple quantum wells are particularized to a stack of asymmetric coupled quantum wells (ACQWs) that provide a "giant" second-order nonlinear optical response over a prescribed band of wavelengths. For example, with a proper choice of wells-and-barriers widths, the quantum theory of N-doped lattice-matched GaP/Si ACQWs predicts a simultaneous photonic resonance of conduction subbands; that is, the 1-2 subband energy separation equals the pump photon energy, while the 1-3 subband separation is the second harmonic (SH) photon energy, thereby leading to strong SH generation. Interestingly, the pump can be filtered out of the PIC for SH propagation in later QW circuit portions after the SH is generated on one part of the circuit.

VI. Superlattice-on-Insulator Circuits

The superlattice functional layer in XOI uses alternating layers of semiconductors A and B—a stack that is then etched into strip waveguides, including ring resonators. We have identified the *undoped*, lattice-matched short-period AB superlattice as a promising SLOI approach to active and passive waveguided PICs-on-insulator: SLOI. There are *m* atomic monolayers (MLs) of semiconductor A and *n* atomic MLs of semiconductor B. That allows us to engineer the SL NLO properties by selecting *m* and *n*. Our approach uses photon-induced valence-to-conduction transitions, which means valence miniband (*vmb*) to conduction miniband (*cmb*) transitions. The lowest energy *vmb-cmb* transition defines the SL transparency zone. Recently, specific predictions have been made [48], [49] for the *vmb-cmb* "resonance-enhanced" NLO responses, including both second- and third-order NLO of the lattice-matched undoped GaP/SL grown in the [111] direction. Very large $\chi^{(2)}$ and Kerr nonlinear index n_2 were found within the 820 nm to 1000 nm wavelength range.

Modern molecular-beam epitaxy (MBE) is the technique of choice for short-period SLs. We propose here that this epitaxy will enable a new range of lattice-matched SLs that are of great interest for SLOI, namely Si/GaP, Si/ZnS, GaP/AlP, 3C-SiC/GaN-z, 3C-SiC/AlN-z, 4H-SiC/AlN-w, GaN/AlN, and Ge/ZnSe. MBE scientists have shown that their technique can be taken to the "layer limit" in which only one or two MLs of each semiconductor are grown in sequence. This thereby opens up the fabrication of "digital alloys," offering the new frontier of "hetero-crystalline layering," meaning that different lattice symmetries for A and B are feasible in a digital alloy. For example, MBE experiments have verified the creation of stable

digital alloys of PbTe with InSb, a rock-salt with zincblende layering [50].

Taking a cue from bonding-experiment results on QWOI, we envision wafer bonding as the process for creating wafer-scale QWOI and SLOI PICs. The stack of layers would be grown (with low defects) upon a handle wafer, after which the exposed stack surface would be bonded to the SiO_2/Si wafer. Then the handle would be etched back to expose the 200-nm stack-on-insulator. Then the monolithic PICs would be etched.

The Pockels effect is an optical phase-shift modulation known as the linear EO effect. It is a second-order NLO effect that can be thought of as an optical sum-frequency generation where one of the input beams is at zero frequency (actually, radio frequency) but with a non-zero electric field. The Pockels effect is powerful in BTO and poled chromophores. However, both approaches rely upon "composite" waveguides such as a-Si/[011]BTO/Si [51] and slotted metal-insulator-metal plasmonic-organic-hybrids [52]. By contrast, the SLOI Pockels-effect PICs deploy simple, monolithic, all-semiconductor strip waveguides. Therefore, it can be argued that EO circuit integration will be easier in the SLOI case while preserving the low-voltage control found in ferroelectrics. The short-period SLs in SLOI offer a significant advance because we find that SL *m, n* engineering can give a large Pockels effect in the layered SL strip. Quite recently, SLOI engineering was performed [53], and the authors found that for a range of wavelengths slightly longer than the valence-band-to–conduction-band SL band edge-wavelength, they predict r_{33} Pockels coefficients that are 5x to 25x larger than r_{33} possessed by "any" compound semiconductor.

This is a new yet-to-be exploited aspect of the novel waveguides in XOIOE wafers. For the wider-gap SLs, our SLOI simulations predict r_{33} in the 50 to 100 pm/V range over the 500 to 700-nm range of visible wavelengths, while Ge/ZnSe offers a similar response for 1550-nm telecom. Electroded SL waveguide circuits will offer fast and low-powered EO modulators and spatial routing switches. This has implications for chip-scale optical computers (both digital and neuromorphic) that utilize a network of broadband 2 x 2 Mach-Zehnder interferometers known as an MZI "mesh" employing EO phase shifters in the MZI arms as well as supplemental EO phase shifters. The SLOI benefit here is that our Pockels approach provides a minimal footprint for each 2 x 2 device, enabling large-scale integration. Optical computing chips often deploy wavelength-division-multiplexed PICs [54], and the lattice-matched SLOI PICs mentioned can drive resonant waveguide structures such as an array of EO microdisks that are side-coupled to passive bus waveguides. In this scenario, the disks and strip waveguides are fabricated from one chosen superlattice. The disks have "miniature" Pockels electrodes to give the desired EO control, such as neural weighting.

VII. Manufacturing the General Xoioe Wafers

We are confident that XOIOE foundry manufacturing on 300-mm Si will come to fruition in the future, but at present, the roadmap to that destination is not entirely defined. Some innovations are needed, along with established techniques. A variety of heterogeneous PIC and OE techniques [59], [60] must be called upon to make the variety of XOIOE wafers.

Wafers of InP and GaAs and 4H-SiC are currently commercially available at 150-mm diameter for bonding to 300-mm Si, but those wafers may become brittle at 300 mm diameters; thus, suppliers may be reluctant to go beyond the 150 mm size. Direct 150-to-300 wafer bonding is practical, but we cannot state that the 300-to-300 bond will be reached.

The "co-packaging" approach is a proven way to form OE circuits. Electronic ICs and photonic ICs are formed on separate wafers (or large chips) with metal contact pads at each top surface. After that, the two ICs are face-to-face bonded, establishing numerous electrical interconnects. That leads to whether practical OEs can be achieved in a side-by-side arrangement of electronics and photonics on one wafer. This ambitious one-package approach will require the development of several 3-dimensional hetero-layering techniques.

For the manufacture of ferroelectric LNOI and BTOI PICs, we note that semiconductor photonics "actives" could be added to the LNOI wafer by die-bonding to LN-removed areas, assuming end-fire coupling between dies and LN waveguides. $BaTiO_3$ is often formed upon a lower-index $SrTiO_3$ layer that rests upon an insulator. According to [35], wafer-bonding is employed to create $BaTiO_3$-on-SOI PICs labeled here as BTOI. CMOS was co-integrated with BTOI [36]. On-wafer PDs can be made with a hetero-method analogous to that in SiPh, where lattice-mismatched Ge is deposited on Si.

Die-bonding is one way to create on-wafer quantum-dot sources, quantum-well laser diodes, combs, and SOAs. Here, chiplets containing those devices are bonded to strategic PIC locations. Such bonding applies to electronic dies as well. Growing these complex active devices on-wafer monolithically is challenging but doable in some cases. Those usually involve an on-oxide buffer or seed layer, plus local-area epitaxy. Some analogous procedures could, in principle, be used for electronics manufacture. As mentioned, CMOS will work well with CSOI.

Having outlined a "universal" XOIOE as a target, we note that current SOI platforms are already useful, accessible, and manufacturable [61]. Between now and the future, technology will be introduced in steps. The ordering matters. Each stage of development must continually impact capabilities rather than address problems that only arise several steps later. This prioritization or roadmap will be bolstered by new techniques to quantifiably compare disparate technologies in photonics, such as their impact on energy-efficient performance [62]. Roadmapping will also rely on forming stakeholder bodies that evaluate payoff against development difficulty, similar to the International Technology Roadmap for Semiconductors (ITRS).

VIII. Speculation on the Future Trajectory of XOIOE

The SOI and SiNOI platforms were established decades ago, as were their on-chip heterogeneous III-V light sources, while LNOI and BTOI arose in the last decade. Some OI developments are relatively recent such as the 2020 layer-transferred AlGaAs-OI waveguides, whose propagation loss is less than 0.2 dB/cm [42]. Other advances such as QWOI and SLOI are presently

awaiting experimental verification, while the various compound-semiconductor-on-insulator approaches that go beyond AlGaAs await foundry manufacture.

Undoubtedly, XOIOE has a bright future, but what will that consist of? If we attempt to predict the future course of XOIOE commercial products and commercial sales, there is the "hazard" that our forecasts could prove to be mostly wrong. Nevertheless, we shall bravely venture some thoughts on the future trajectory.

XOIOE laser light sources can be on-chip or off-chip, but our opinion is that on-chip will dominate in the future. This could happen by expanding vendors offering foundry back-end processing options to add III-V lasers-and-SOAs to chips or by creating these key elements at the wafer scale. We guess that wafer-scale will dominate due to its cost-effectiveness, although the device reliability, test, and yield are open questions for wafers.

A few years ago, it appeared that the photonics community was set to consolidate on the SOI platform. However, recently there has been evidence that the situation is changing, and that people are presently favoring SiNOI, such as the low-loss waveguiding platform described by the trade name TriPlex [63]. SiNOI offers impressive features: wavelength coverage of 405 nm through mid-infrared, easy interfacing with single-mode fibers, relatively high index contrast between nitride and oxide (1.98 versus 1.45), and PIC manufacture in a single monolithic process flow where standard building blocks are combined to build the complex circuit. Thermo-optic and stress-optic phase shifting are available. Most important is hybrid SiNOI integration with III-V lasers, detectors, and modulators.

In our opinion, there will likely continue to be convergence onto SiNOI, with this platform taking a significant fraction of sales. However, we feel that it is unlikely that there will be an industry "shakeout" in which a single platform comes to dominate all the other platforms. The reason is that the XOIOE applications space is vast, and thus a diversity of platform approaches is needed to "satisfy that space." For example, in the area of dense WDM optical communications transceivers, the SOI platform is a capable and strong performer. Recent work [64] centered at 1325 nm shows that the heterogeneous integration of an InAs/GaAs frequency-comb laser on the SOI, together with GaAs/Si MOSCAP modulators and SiGe APDs provides excellent energy-efficient 40-channel communications.

The recent low-loss waveguiding results for AlGaAsOI are an "existence theorem," indicating that the transition to foundry manufacture will be successful for this system and other III-V and II-VI OI wafers.

The current popularity of LNOI could fade due to superior metrics offered by the newer BTOI platforms, for example, in the metrics of footprint and voltage required.

In the future, industries related to communications, sensing, computing, LIDAR, and quantum photonics will drive the different types of XOIOE solutions; also, there will be significant industry drivers that have very little presence today. In other words, it is difficult to predict the full list of industry drivers and to foretell which drivers shall be primary and which minor.

We expect huge sales volumes for these XOIOE chips, but we do not feel that such OE volumes will approach the current volumes for CMOS electronics. Some recent reviews [65], [66], [67], [68], [69], [70] help to illuminate the future opportunities and tasks of XOIOE.

IX. Summary

The 300-mm Si-based "universal" XOIOE wafer offers many combinations of readily available and numerous pho-tonic integrated-circuit materials (in several materials families) that are heterogeneously integrated on-wafer, and the symbol "X" refers to a specific combination chosen by the wafer user. For the optoelectronic OE aspect, several kinds of transistor-electronic circuits can be integrated on-wafer to work harmoniously with the photonics, with CMOS being the primary electronics and with BiCMOS, HBTs, HEMTs, and MESFETs also available for co-integration. As to applications, the general XOIOE will essentially fulfill all key waveguided classical-and quantum-optoelectronic- chip applications and a host of important free-space OE applications. The vast XOIOE applications range is due to the diverse and highly competent performances offered by the wide range of X-materials that includes the group-IV, III- V, II-VI semiconductors, silicon-nitride, Ta_2O_5 and diamond insulators, ferroelectric $BaTiO_3$, $KNbO_2$, $LiNbO_3$, the various poled organic polymers, phase-change materials, plasmonics, 2D graphene, and MEMs-structured materials. Nano-layered semiconductor waveguides (especially lattice-matched short-period superlattice waveguides) are a new category of "man-made semiconductors" that offer enhanced nonlinear and electro-optical effects.

A photonics user would select a particular X that meets his specific needs, although a switching network on-wafer could reconfigure the PICs to target different applications. It is within the present foundry art to create high-performance laser diodes, semiconductor optical amplifiers, photodetectors, switches, and modulators on-wafer, and the high-volume manufacture of XOIOEs is judged to be feasible; however, many aspects, such as detailed 3D hetero-integration processes, are not known yet, and overall, the foundry development is still in a reasonably early stage.

References

[1] J. M. Shainline, "Optoelectronic intelligence," *Appl. Phys. Lett.*, vol. 118, no. 16, 2021, Art. no. 160501, doi: 10.1063/5.0040567.

[2] H. Xu et al., "Design and synthesis of chromophores with enhanced electro-optic activities in both bulk and plasmonic–organic hybrid devices," *Mater. Horiz.*, vol. 9, pp. 261–270, 2022, doi: 10.1039/D1MH01206A.

[3] M. Wuttig, H. Bhaskaran, and T. Taubner, "Phase-change materials for non-volatile photonic applications," *Nature Photon.*, vol. 11, no. 8, pp. 465–476, 2017, doi: 10.1038/nphoton.2017.126.

[4] D. Moor et al., "150 GHz hybrid-plasmonic $BaTiO_3$-On-SOI modulator for CMOS foundry integration," in *Proc. Front. Opt. + Laser Sci. Optica Publishing Group*, 2021, Art. no. FTh4D.2. [Online]. Available: http://opg.optica.org/abstract.cfm?URI=FiO-2021-FTh4D.2

[5] R. Amin et al., "Heterogeneously integrated ITO plasmonic Mach–Zehnder interferometric modulator on SOI," *Sci. Rep.*, vol. 11, no. 1, 2021, Art. no. 1287, doi: 10.1038/s41598-020-80381-3.

[6] J. Liu, Z. U. Khan, C. Wang, H. Zhang, and S. Sarjoghian, "Review of graphene modulators from the low to the high figure of merits," *J. Phys. D: Appl. Phys.*, vol. 53, no. 23, Apr. 2020, Art. no. 233002, doi: 10.1088/1361-6463/ab7cf6.

[7] B. J. Shastri et al., "Photonics for artificial intelligence and neuromorphic computing," *Nature Photon.*, vol. 15, no. 2, pp. 102–114, 2021, doi: 10.1038/s41566-020-00754-y.

[8] P. R. Prucnal, B. J. Shastri, and M. C. Teich, *Neuromorphic Photonics*. Boca Raton, FL, USA: CRC Press, 2017.

[9] Z. Ying et al., "Sequential logic and pipelining in chip-based electronic-photonic digital computing," *IEEE Photon. J.*, vol. 12, no. 6, Dec. 2020, Art. no. 7801311.

[10] L. Larger et al., "Photonic information processing beyond turing: An optoelectronic implementation of reservoir computing," *Opt. Exp.*, vol. 20, no. 3, pp. 3241–3249, Jan. 2012. [Online]. Available: http://opg.optica.org/oe/abstract.cfm?URI=oe-20-3-3241

[11] G. V. der Sande, D. Brunner, and M. C. Soriano, "Advances in photonic reservoir computing," *Nanophotonics*, vol. 6, no. 3, pp. 561–576, 2017, doi: 10.1515/nanoph-2016-0132.

[12] T. Inagaki et al., "A coherent Ising machine for 2000-node optimization problems," *Science*, vol. 354, no. 6312, pp. 603–606, 2016, doi: 10.1126/science.aah4243.

[13] A. Marandi, Z. Wang, K. Takata, R. L. Byer, and Y. Yamamoto, "Network of time-multiplexed optical parametric oscillators as a coherent Ising machine," *Nature Photon.*, vol. 8, no. 12, pp. 937–942, 2014, doi: 10.1038/nphoton.2014.249.

[14] Z. Cheng et al., "Device-level photonic memories and logic applications using phase-change materials," *Adv. Mater.*, vol. 30, no. 32, pp. 1802435, 2018, doi: 10.1002/adma.201802435.

[15] E. Kuramochi et al., "Large-scale integration of wavelength-addressable all-optical memories on a photonic crystal chip," *Nature Photon.*, vol. 8, no. 6, pp. 474–481, 2014, doi: 10.1038/nphoton.2014.93.

[16] W. J. Bock and G. Xiao, *Photonic Sensing: Principles and Applications For Safety and Security Monitoring*. New York, NY, USA: Wiley, 2012.

[17] G. Moody et al., "2022 roadmap on integrated quantum photonics," *J. Phys.: Photon.*, vol. 4, no. 1, Jan. 2022, Art. no. 012501, doi: 10.1088/2515-7647/ac1ef4.

[18] V. Giovannetti, S. Lloyd, and L. Maccone, "Advances in quantum metrology," *Nature Photon.*, vol. 5, no. 4, pp. 222–229, 2011, doi: 10.1038/nphoton.2011.35.

[19] D. Marpaung, J. Yao, and J. Capmany, "Integrated microwave photonics," *Nature Photon.*, vol. 13, no. 2, pp. 80–90, 2019, doi: 10.1038/s41566-018-0310-5.

[20] K. Ahi, N. Jessurun, M.-P. Hosseini, and N. Asadizanjani, "Survey of terahertz photonics and biophotonics," *Opt. Eng.*, vol. 59, no. 6, pp. 1–31, 2020, doi: 10.1117/1.OE.59.6.061629.

[21] X. Guan et al., "Silicon photonics in optical access networks for 5G communications," *IEEE Commun. Mag.,* vol. 59, no. 6, pp. 126–131, Jan. 2021.

[22] Z.-Q. Yan et al., "Underwater photon-inter-correlation optical communication," *Photon. Res.*, vol. 9, no. 12, pp. 2360–2368, Dec. 2021. [Online]. Available: http://opg.optica.org/prj/abstract.cfm?URI=prj-9-12-2360

[23] Q. Shi et al., "Progress in wearable electronics/photonics—Moving toward the era of artificial intelligence and internet of things," *InfoMat*, vol. 2, no. 6, pp. 1131–1162, 2020.

[24] T. J. Kippenberg, A. L. Gaeta, M. Lipson, and M. L. Gorodetsky, "Dissipative Kerr solitons in optical microresonators," *Science*, vol. 361, no. 6402, 2018, Art. no. eaan8083. [Online]. Available: https://www.science.org/doi/abs/10.1126/science.aan8083

[25] R. Amin et al., "ITO-based electro-absorption modulator for photonic neural activation function," *APL Mater.*, vol. 7, no. 8, 2019, Art. no. 081112, doi: 10.1063/1.5109039.

[26] A. N. Tait et al., "Silicon photonic modulator neuron," *Phys. Rev. Appl.*, vol. 11, Jun. 2019, Art. no. 064043, doi: 10.1103/PhysRevApplied.11.064043.

[27] F. De Leonardis, B. Troia, R. A. Soref, and V. M. N. Passaro, "Dispersion of nonresonant third-order nonlinearities in GeSiSn ternary alloys," *Sci. Rep.*, vol. 6, no. 1, 2016, Art. no. 32622, doi: 10.1038/srep32622.

[28] A. Honardoost, J. Henriksson, K. Kwon, J. Luo, and M. C. Wu, "Low-loss wafer-bonded silicon photonic MEMs switches," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, 2022, pp. 1–3. [Online]. Available: http://opg.optica.org/abstract.cfm?URI=OFC-2022-M2D.8

[29] X. Zhang, K. Kwon, J. Henriksson, J. Luo, and M. C. Wu, "A large- scale microelectromechanical-systems-based silicon photonics LiDAR," *Nature*, vol. 603, no. 7900, pp. 253–258, 2022, doi: 10.1038/s41586-022-04415-8.

[30] X. Mei et al., "First demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015.

[31] Y. Zhou et al., "Electrically injected GeSn lasers with peak wavelength up to 2.7 μm," *Photon. Res.*, vol. 10, no. 1, pp. 222–229, Jan. 2022. [Online]. Available: http://opg.optica.org/prj/abstract.cfm?URI=prj-10-1-222

[32] S. Mi, M. Kiss, T. Graziosi, and N. Quack, "Integrated photonic devices in single crystal diamond," *J. Phys.: Photon.*, vol. 2, no. 4, Aug. 2020, Art. no. 042001, doi: 10.1088/2515-7647/aba171.

[33] A. Yi et al., "Silicon carbide for integrated photonics," *Appl. Phys. Rev.*, vol. 9, 2022, Art. no. 031302.

[34] A. Shams-Ansari et al., "Reduced material loss in thin-film lithium niobate waveguides," *APL Photon.*, vol. 7, 2022, Art. no. 081301.

[35] L. Czornomaz and S. Abel, "BTO-enhanced silicon photonics – a scalable PIC platform with ultra-efficient electro-optical modulation," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, 2022, pp. 1–3.

[36] B. Chen et al., "Signatures of enhanced out-of-plane polarization in asymmetric $BaTiO_3$ superlattices integrated on silicon," *Nature Commun.*, vol. 13, no. 1, 2022, Art. no. 265, doi: 10.1038/s41467-021-27898-x.

[37] S. Abel, "An ultra-strong Pockels effect in silicon photonics," *Proc. SPIE*, vol. 11690, 2021, Art. no. 116900Y, doi: 10.1117/12.2591232.

[38] C. Wang et al., "High-Q microresonators on 4H-silicon-carbide- on-insulator platform for nonlinear photonics," *Light: Sci. Appl.*, vol. 10, no. 1, 2021, Art. no. 139, doi: 10.1038/s41377-021-00584-9.

[39] M. Soltani, R. Soref, T. Palacios, and D. Englund, "AlGaN/AlN integrated photonics platform for the ultraviolet and visible spectral range," *Opt. Exp.*, vol. 24, no. 22, pp. 25415–25423, Oct. 2016.

[40] T. Fujii, T. Sato, K. Takeda, T. Kakitsuka, and S. Matsuo, "Epitaxial growth technique using InP-on-insulator towards III-V/Si photonic integrated circuits," in *Proc. JSAP-OSA Joint Symposia 2019 Abstr.*, 2019, Paper 20a E215 1.

[41] Z. Yan et al., "A monolithic InP/SOI platform for integrated photonics," *Light: Sci. Appl.*, vol. 10, no. 1, 2021, Art. no. 200, doi: 10.1038/s41377-021-00636-0.

[42] L. Chang, G. D. Cole, G. Moody, and J. E. Bowers, "CSOI: Beyond silicon-on-insulator photonics," *Opt. Photon. News*, vol. 33, no. 1, pp. 24–31, 2022.

[43] M. R. Billah et al., "Hybrid integration of silicon photonics circuits and InP lasers by photonic wire bonding," *Optica*, vol. 5, no. 7, pp. 876–883, Jul. 2018. [Online]. Available: http://opg.optica.org/optica/abstract.cfm?URI=optica-5-7-876

[44] C. Sun et al., "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, no. 7583, pp. 534–538, 2015, doi: 10.1038/nature16454.

[45] Y. Zhu et al., "Hybrid integration of deterministic quantum dots-based single-photon sources with CMOS-compatible silicon carbide photonics," 2022, *arxiv.org/abs/2203.12202*.

[46] D. Colucci et al., "Unique design approach to realize an O-band laser monolithically integrated on 300-mm Si substrate by nano-ridge engineering," *Opt. Exp.*, vol. 30, no. 8, pp. 13510–13521, Apr. 2022. [Online]. Available: http://opg.optica.org/oe/abstract.cfm?URI=oe-30-8-13510

[47] F. De Leonardis and R. A. Soref, "Efficient second-harmonic generation in Si/GaP asymmetric coupled-quantum-well waveguides," *J. Lightw. Technol.*, vol. 40, no. 9, pp. 2959–2964, May 2022.

[48] F. De Leonardis and R. Soref, "Harmonic generation in GaP/Si and GaP/AlP superlattice-based waveguides," *J. Lightw. Technol.*, vol. 40, no. 16, pp. 5646–5653, Aug. 2022.

[49] R. Soref and F. De Leonardis, "Classical and quantum photonic sources based on nonlinear Gap/Si-superlattice micro-ring resonators," *Chip J.*, 2022, Art. no. 100011, doi: 10.1016/j.chip.2022.100011.

[50] M. B. Lassise, T. T. McCarthy, B. D. Tracy, D. J. Smith, and Y.-H. Zhang, "Molecular beam epitaxial growth and structural properties of hetero-crystalline and heterovalent PbTe/CdTe/InSb structures," *J. Appl. Phys.*, vol. 126, no. 4, 2019, Art. no. 045708, doi: 10.1063/1.5097276.

[51] A. Karvounis, F. Timpu, V. V. Vogler-Neuling, R. Savo, and R. Grange, "Barium titanate nanostructures and thin films for photonics," *Adv. Opt. Mater.*, vol. 8, no. 24, 2020, Art. no. 2001249. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adom.202001249

[52] W. Heni et al., "Silicon-organic and plasmonic-organic hybrid photonics," *ACS Photon.*, vol. 4, no. 7, pp. 1576–1590, 2017, doi: 10.1021/acsphotonics.7b00224.

[53] F. De Leonardis and R. Soref, "High-performance Pockels—Effect modulation and switching in silicon-based GaP/Si, AlP/Si, ZnS/Si, AlN/3C-SiC, GaaS/Ge, ZnSe/GaAs, and ZnSe/Ge superlattice-on-insulator integrated circuits," *Sensors J.*, to be published.
[54] A. Tait et al., "Neuromorphic photonic networks using silicon photonic weight banks," *Sci. Rep.*, vol. 7, 2017, Art. no. 12.
[55] R. Soref and B. Bennett, "Electrooptical effects in silicon," *IEEE J. Quantum Electron.*, vol. 23, no. 1, pp. 123–129, Jan. 1987.
[56] T. Hiraki et al., "Heterogeneously integrated III-V/Si MOS capacitor Mach–Zehnder modulator," *Nature Photon.*, vol. 11, no. 8, pp. 482–485, 2017, doi: 10.1038/nphoton.2017.120.
[57] C. Ye, K. Liu, R. A. Soref, and V. J. Sorger, "A compact plasmonic MOS-based 2×2 electro-optic switch," *Nanophotonics*, vol. 4, no. 3, pp. 261–268, 2015, doi: 10.1515/nanoph-2015-0010.
[58] J. Sun, W. Wang, and Z. Li, "A CMOS-compatible carrier-injection plasmonic micro-ring modulator with resonance tuning by carrier concentration," *Photonics*, vol. 9, no. 5, 2022, Art. no. 272. [Online]. Available: https://www.mdpi.com/2304-6732/9/5/272
[59] L. De Marinis, M. Cococcioni, P. Castoldi, and N. Andriolli, "Photonic neural networks: A survey," *IEEE Access*, vol. 7, pp. 175827–175841, 2019.
[60] L. El Srouji et al., "Photonic and optoelectronic neuromorphic computing," *APL Photon.*, vol. 7, no. 5, 2022, Art. no. 051101, doi: 10.1063/5.0072090.
[61] A. Yariv and P. Yeh, *Photonics: Optical Electronics in Modern Communications*. Oxford, U.K.: Oxford Univ. Press, 2007.
[62] A. N. Tait, "Quantifying power in silicon photonic neural networks," *Phys. Rev. Appl.*, vol. 17, May 2022, Art. no. 054029, doi: 10.1103/PhysRevApplied.17.054029.
[63] C. G. H. Roeloffzen et al., "Low-loss Si_3N_4 TriPlexX optical waveguides: Technology and applications overview," *IEEE J. Sel. Topics Quantum Electron.*, vol. 24, no. 4, Jul./Aug. 2018, Art. no. 4400321.
[64] D. Liang et al., "An energy-efficient and bandwidth-scalable DWDM heterogeneous silicon photonics integration platform," *IEEE J. Sel. Topics Quantum Electron.*, vol. 28, no. 6, Nov./Dec. 2022, Art. no. 610081.
[65] I. A. Fisher et al., "On-chip infrared photonics with Si-Ge heterostructures: What is next?," *APL Photon.*, vol. 7, 2022, Art. no. 050901.
[66] J. C. Adcock et al., "Advances in silicon quantum photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 27, no. 2, Mar./Apr. 2021, Art. no. 6700224.
[67] C. Xiang et al., "High-performance silicon photonics using heterogeneous integration," *IEEE J. Sel. Topics Quantum Electron.*, vol. 28, no. 3, May/Jun. 2022, Art. no. 8200515.
[68] M. Li et al., "Quantum microwave photonics," *IEEE J. Lightw. Technol.*, early access, May 20, 2022, doi: 10.1109/JLT.2022.3176303.
[69] A. Mai, P. Steglich, C. Mai, S. Simon, and R. Scholz, "Electronic-photonic Wafer-level technologies for fast prototyping and application-specific solutions," in *Proc. Photon. Electromagnetics Res. Symp. Spring*, 2019, pp. 249–255.
[70] C. Y. Hsu, G. Z. Yiu, and Y. C. Chang, "Free-space applications of silicon photonics: A review," *Micromachines MDPI*, vol. 13, 2022, Art. no. 990.

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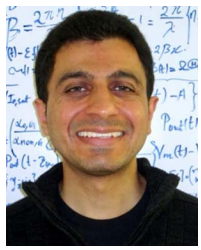

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