Truly Modular Burst-Mode CDR With Instantaneous Phase Acquisition for Multiaccess Networks

Bhavin J. Shastri, *Student Member, IEEE*, and David V. Plant, *Fellow, IEEE*

***Abstract*— We demonstrate a novel 10-Gb/s burst-mode clock and data recovery circuit (BM-CDR) for multiaccess networks. Our design is based on a hybrid topology of a feedback CDR and a feed-forward clock phase aligner utilizing space-sampled clocks. The BM-CDR achieves a bit error rate (BER) $< 10^{-10}$ while featuring instantaneous (0-bit) phase acquisition for any phase step ($\pm 2\pi$ rad) between successive bursts. We also develop a probabilistic theoretical model for space-sampled BM-CDRs to quantify the BER performance. The theoretical model accounts for the phase step between consecutive packets, packet preamble length, and jitter on the sampling clock.**

***Index Terms*— Burst-mode, clock and data recovery, clock phase aligner, probabilistic theory, space sampling.**

I. Introduction

AS THE explosive growth in Internet traffic continues, the need for highly-specialized low-cost integrated circuits is undeniable, with clock and data recovery (CDR) being a critical function in back plane routing and chip-to-chip interconnects. Furthermore, the traffic received on these multiaccess links—passive optical networks [1] and packet-switched networks [2]—is inherently bursty with asynchronous phase steps $|\Delta\varphi| \leq 2\pi$ rad, that exist between the consecutive k^{th} and $(k+1)^{\text{th}}$ packets. This inevitably causes conventional CDR circuits to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDR feedback loop enough time to settle down and thus acquire lock. However, the use of a preamble reduces the effective throughput and increases delay. Consequently, to deal with bursty data, these networks require a burst-mode CDR (BM-CDR). Different approaches have been proposed to build BM-CDRs with short phase acquisition times—the most important characteristic. The first approach, based on feedback, consists in increasing the bandwidth of a phase-locked loop (PLL)-based CDR to reduce the settling time [3]. The disadvantages include stability issues, jitter peaking, and limited jitter filtering. The second approach, based on feed-forward, consists of gated oscillators [4]. Here, clock phase alignment is done by triggering the local clock on each transition of the input. Phase acquisition is rapid, but this solution is susceptible to pulse distortions and does not filter out input jitter. The last approach is based on time oversampling [1], [2] which requires electronics operating at twice or thrice the aggregate bit rate resulting in wasted power, in addition to the knowledge of a predefined unique delimiter (start of packet) that is exploited as a signature for phase picking. In this letter, we present a novel BM-CDR architecture based on space sampling with a hybrid topology of feedback and feed-forward. The BM-CDR uses electronics operated *at* the bit rate with *no a priori* knowledge of the delimiter, leading to more efficient power consumption and being truly modular across application testbeds, respectively. The 10-Gb/s BM-CDR achieves a bit error rate (BER) $< 10^{-10}$ with instantaneous (0-bit) phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad, between consecutive bits. We also develop a probabilistic theoretical model for space-sampled BM-CDRs to quantify the BER performance while accounting for phase steps between successive packets, preamble length, and jitter on the sampling clock.

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The authors are with the Photonic Systems Group, Department of Electrical and Computer Engineering, McGill University, Montreal, QC H3A 2A7, Canada (e-mail: shastri@ieee.org; david.plant@mcgill.ca).

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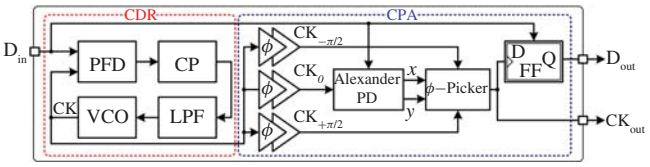

Fig. 1. Block diagram of BM-CDR architecture.

II. Novel BM-CDR Architecture

A block diagram of the proposed BM-CDR is shown in Fig. 1. The BM-CDR is composed of a phase-tracking CDR and a clock phase aligner (CPA). The CDR senses data D_{in}, and generates a synchronized clock CK, with a voltage-controlled oscillator (VCO) in a PLL (feedback). The phase and frequency of CK is compared to D_{in} in the phase/frequency detector (PFD), generating an error signal that is passed through the charge pump (CP) and the low-pass filter (LPF) to set the voltage required by the VCO to oscillate at the frequency of interest. Thereafter the CPA (feed-forward) utilizes multi-phase clocks and a phase picking algorithm based on an "early-late" detection principle. The CPA is comprised of phase (ϕ-) shifters, an Alexander phase detector (PD), a ϕ-picker, and a D flip-flop (D-FF). The ϕ-shifters utilize the clock recovered by the CDR CK, to provide multiple clocks: CK_o, $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases: 0 rad, $-\pi/2$ rad, and $+\pi/2$ rad, respectively, with respect to CK. Next, an Alexander PD [5] which inherently

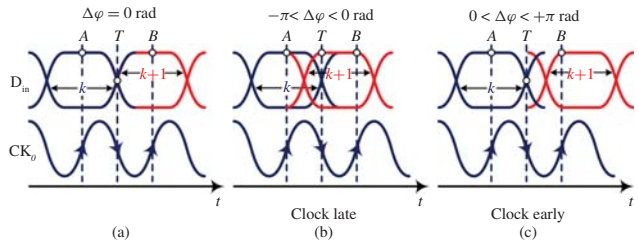

Fig. 2. (a) Three-point sampling scheme. (b) and (c) Early-late waveforms.

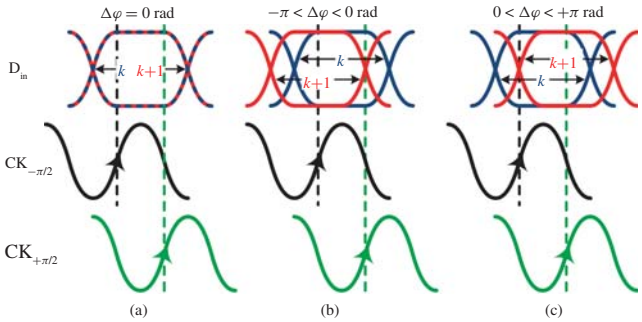

Fig. 3. CPA phase picking algorithm. Three different phase steps are considered: (a) $\Delta\varphi = 0$ rad; (b) $-\pi < \Delta\varphi < 0$ rad; and (c) $0 < \Delta\varphi < +\pi$ rad.

exhibits *bang-bang* (binary) characteristics is used to strobe the data waveform D_{in}, with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions [see Fig. 2(a)], resulting in three data samples: previous bit A, current bit B, and a sample of the current bit at the zero crossing T. Depending on the phase difference between the consecutive packets, the PD aided by these samples, $X \equiv T \oplus B$ and $Y \equiv A \oplus T$, can determine the location of the clock edge with respect to the data edge as follows: (a) if $A \neq T = B$ ($X \downarrow$, $Y \uparrow$) $\Rightarrow$ CK_o lags D_{in}—is late—when $-\pi < \Delta\varphi < 0$ rad [see Fig. 2(b)]; (b) if $A = T \neq B$ ($X \uparrow$, $Y \downarrow$) $\Rightarrow$ CK_o leads D_{in}—is early—when $0 < \Delta\varphi < +\pi$ rad [see Fig. 2(c)]; (c) if $A = T = B$ ($X \downarrow$, $Y \downarrow$) $\Rightarrow$ no data transition is present due to consecutive identical digits (CIDs); and (d) if $A = B \neq T$ ($X \uparrow$, $Y \uparrow$) $\Rightarrow$ no decision is possible. The clock CK_o early-late information (X and Y) together with the two multi-phase clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, is provided to the ϕ-picker.

The idea behind the phase picking algorithm is depicted with the aid of eye diagrams in Fig. 3. When there is no phase difference between the consecutive packets, $\Delta\varphi = 0$ rad, either of the clocks, $CK_{-\pi/2}$ and $CK_{+\pi/2}$, will correctly sample the data bits of the phase shifted $(k+1)^{\text{th}}$ packet [see Fig. 3(a)]. This is also true for an antiphase step $\Delta\varphi = \pm\pi$ rad—not shown as this is a modulo-π process. For a phase step $-\pi < \Delta\varphi < 0$ rad, clock $CK_{+\pi/2}$ will sample the bits on or close to the transitions of the data eye, whereas clock $CK_{-\pi/2}$ will correctly sample the data [see Fig. 3(b)]. Similarly for a phase step $0 < \Delta\varphi < +\pi$ rad, clock $CK_{-\pi/2}$ will sample the bits on or close to the transitions, whereas clock $CK_{+\pi/2}$ will correctly sample the data [see Fig. 3(c)]. That is, regardless of any phase step, there will be at least one clock, either $CK_{-\pi/2}$ or $CK_{+\pi/2}$, that will yield an accurate

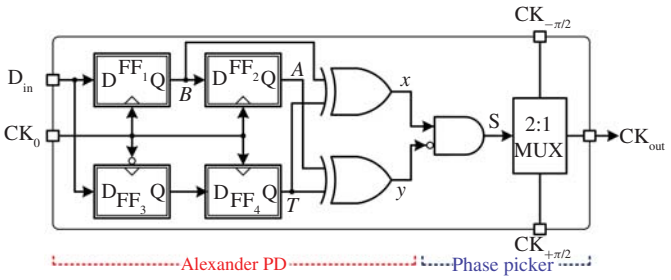

Fig. 4. Hardware implementation of Alexander PD and ϕ-picker.

sample. The ϕ-picker then selects the most accurate clock CK_{out}, from these two possibilities for driving the D-FF to sample the noisy data (retime) yielding an output D_{out} with less jitter. The foregoing concepts on the Alexander PD and ϕ-picker lead to the circuit topology in Fig. 4.

III. Probabilistic Theory

The sampling error probability of the CDR in presence of phase steps $|\Delta\varphi| \leq 2\pi$ rad, and an l-bit preamble is [1]

$$P_s\left(|\Delta\varphi|, l\right) = \frac{1}{2}Q\left(\frac{\pi - \widetilde{\psi}}{2\pi\,\sigma_{t_s}[\text{UI}]}\right) + \frac{1}{2}Q\left(\frac{\pi + \widetilde{\psi}}{2\pi\,\sigma_{t_s}[\text{UI}]}\right) \quad (1)$$

where $\widetilde{\psi} = \left(|\Delta\varphi| - \psi\right) \times \left(1 - \eta(l)\right)$, $\eta(l)$ measures the CDRs lock acquisition time [1], σ_{t_s} is the root mean square (rms) jitter on the sampling clock in unit interval (UI), $(\psi, \Delta\varphi) \in \left\{\left(0, [-\pi, +\pi]\right), \left(2\pi, [\pm\pi, \pm 2\pi]\right)\right\}$, and $Q(x) \triangleq \left(1/\sqrt{2\pi}\right)\int_x^\infty \exp\left(-\lambda^2/2\right) d\lambda$ is the normalized Gaussian tail probability. Moving forward, the Alexander PDs probability of correctly determining an early/late clock can be written as

$$\Pr\left(CK_o\right) = \Pr\left(A\right) \times \Pr\left(B\right) \times \Pr\left(T\right) \quad (2)$$

and the probabilities of correctly sampling the points A, B, and T, can be given as:

$$\Pr\left(A\right) = \Pr\left(B\right) \times \left[1 - P_s\left(|\Delta\varphi|\right)\right] \quad (3)$$

$$\Pr\left(B\right) = 1 - P_s\left(|\Delta\varphi|\right) \quad (4)$$

$$\Pr\left(T\right) = \Pr(\widetilde{T}) \times \left[1 - P_s\left(|\Delta\varphi|\right)\right] \quad (5)$$

$$\Pr(\widetilde{T}) = 1 - \vartheta\left[P_s\left(|\Delta\varphi| - \pi\right) + P_s\left(|\Delta\varphi| + \pi\right)\right] \quad (6)$$

where $P_s\left(|\Delta\varphi|\right) = P_s\left(|\Delta\varphi|, l = 0\right)$ sampling error probability of a bit, and $(\vartheta, \Delta\varphi) \in \left\{\left(0.5, [-\pi, +\pi]\right), \left(1, [\pm\pi, \pm 2\pi]\right)\right\}$. Consequently, for the BM-CDR based on space sampling and the CPA, the sampling error probability is expressed as

$$P_s^{\text{BM-CDR}} = \Pr\left(CK_o\right) \times \min\left\{P_s\left(|\Delta\varphi| - t_k\right)\right\} \quad (7)$$

where $t_k = \pm\pi/2$ are the sampling points for the multi-phase clocks $CK_{-\pi/2}$ or $CK_{+\pi/2}$.

IV. Results and Discussion

The BM-CDR is built from commercially available low cost/complexity electronics rated at 13 Gb/s. The CDR is from Centellax (TR1C1-A) and the CPA is built by integrating Hittite Microwave evaluation boards: ϕ-shifters (HMC538LP4),

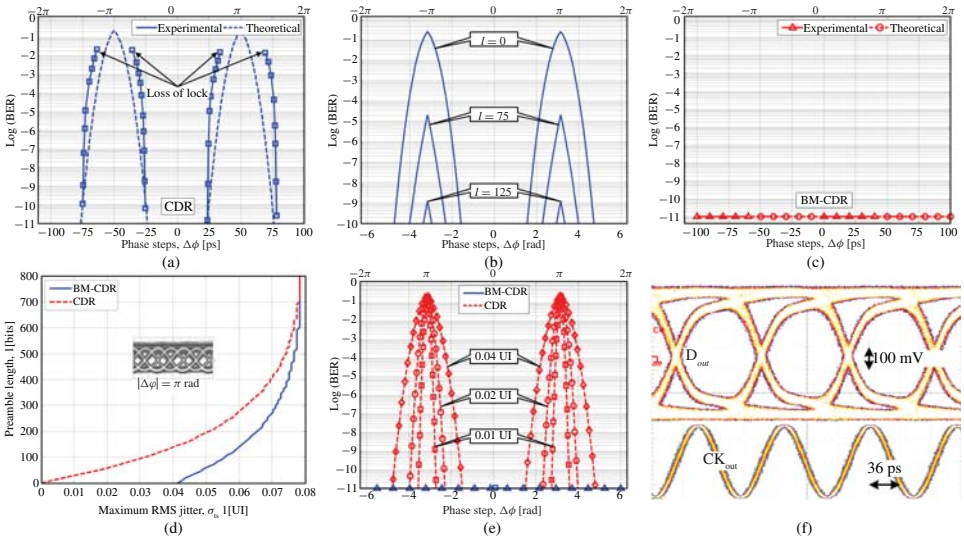

Fig. 5. BER performance versus phase step for zero preamble length. (a) CDR. (b) CDR performance with increasing preamble length. (c) BM-CDR. (d) Preamble length versus rms jitter to achieve BER $< 10^{-10}$ for worst-case phase step $|\Delta\varphi| = \pi$ rad. (e) Effect of rms jitter. (f) Recovered data and clock.

Alexander PD (HMC6032LC4B), AND gate (HMC672LC3C), 2:1 selector (HMC748LC3C), and D-FF (HMC673LC3C).

The BM-CDR is tested using a standard burst-mode test setup [3]. Fig. 5(a) shows the experimental BER performance of the CDR at 10 Gb/s as a function of the phase step between two consecutive data bits, for a zero preamble length. As expected, the worst-case phase steps are around ± 50 ps because these represent the half-bit periods ($\pm\pi$ rad), and therefore the CDR is sampling near the edges of the data eye, resulting in a loss of lock. At relatively small phase shifts (near 0 or $\pm 2\pi$ rad), we can easily achieve error-free operation, BER $< 10^{-10}$, because the CDR is almost sampling at the middle of each data bit. To measure the phase acquisition time of the CDR, preamble bits ("1010$\cdots$"pattern) can be inserted at the beginning of the packet to help the PLL of the CDR to settle down and acquire lock until error-free operation is achieved. In Fig. 5(b), as the preamble length is increased, there is an improvement in the BER. After 125 preamble bits we perceive error-free operation for any phase step. However, the use of a preamble introduces overhead, reducing the effective throughput and increasing delay. For the proposed BM-CDR as depicted in Fig. 5(c), we achieve error-free operation for any phase step $|\Delta\varphi| \leq 2\pi$ rad with *zero* preamble bits allowing for instantaneous phase acquisition. The experimental results are in close agreement with the theoretical predictions in Figs. 5(a) and (c). For the CDR, the theoretical bound is optimistic for BER $> 10^{-6}$ as the probabilistic model accounts for the jitter input to the receiver and not for jitter generated by the circuitry; for example, VCO phase noise. Fig. 5(d) shows the number of preamble bits required by the BM-CDR and CDR to obtain a BER $\leq 10^{-10}$ as a function of maximum allowable rms jitter for the worst case phase step $|\Delta\varphi| = \pi$ rad. The proposed BM-CDR is able to achieve instantaneous phase acquisition ($l = 0$) when the rms jitter $\sigma_{t_s} \leq 0.04$ UI; this is true for any phase step $|\Delta\varphi| \leq 2\pi$ rad. However, it is not feasible for the CDR to achieve instantaneous phase acquisition as a jitter-free signal $\sigma_{t_s}^{\max} = 0$ UI, is practically impossible. As a function of phase steps, Fig. 5(e) plots the BER performance for different rms jitter and zero preamble bits. Whereas the BM-CDR achieves instantaneous phase acquisition for any phase step when rms jitter $\sigma_{t_s} \leq 0.04$ UI, the CDR performance degrades with increasing rms jitter. Fig. 5(f) shows the eye diagram of the recovered data and clock in response to a $2^{15} - 1$ PRBS pattern. The rms jitter of the recovered clock is 2.5 ps. The response to CIDs is similar to that in [1].

V. Conclusion

We have demonstrated a novel BM-CDR architecture based on space sampling that achieves instantaneous phase acquisition which can be used to increase the network's: power budget by reducing the burst-mode sensitivity penalty; or effective throughput by increasing the information rate. Our eloquent, scalable architecture leverages the design of low complexity commercial electronics, providing a cost-effective solution. We have also developed a probabilistic theory for space-sampled BM-CDRs validated by the experimental results. This model can refine theoretical models of multiaccess networks and provide input for establishing realistic power budgets.

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